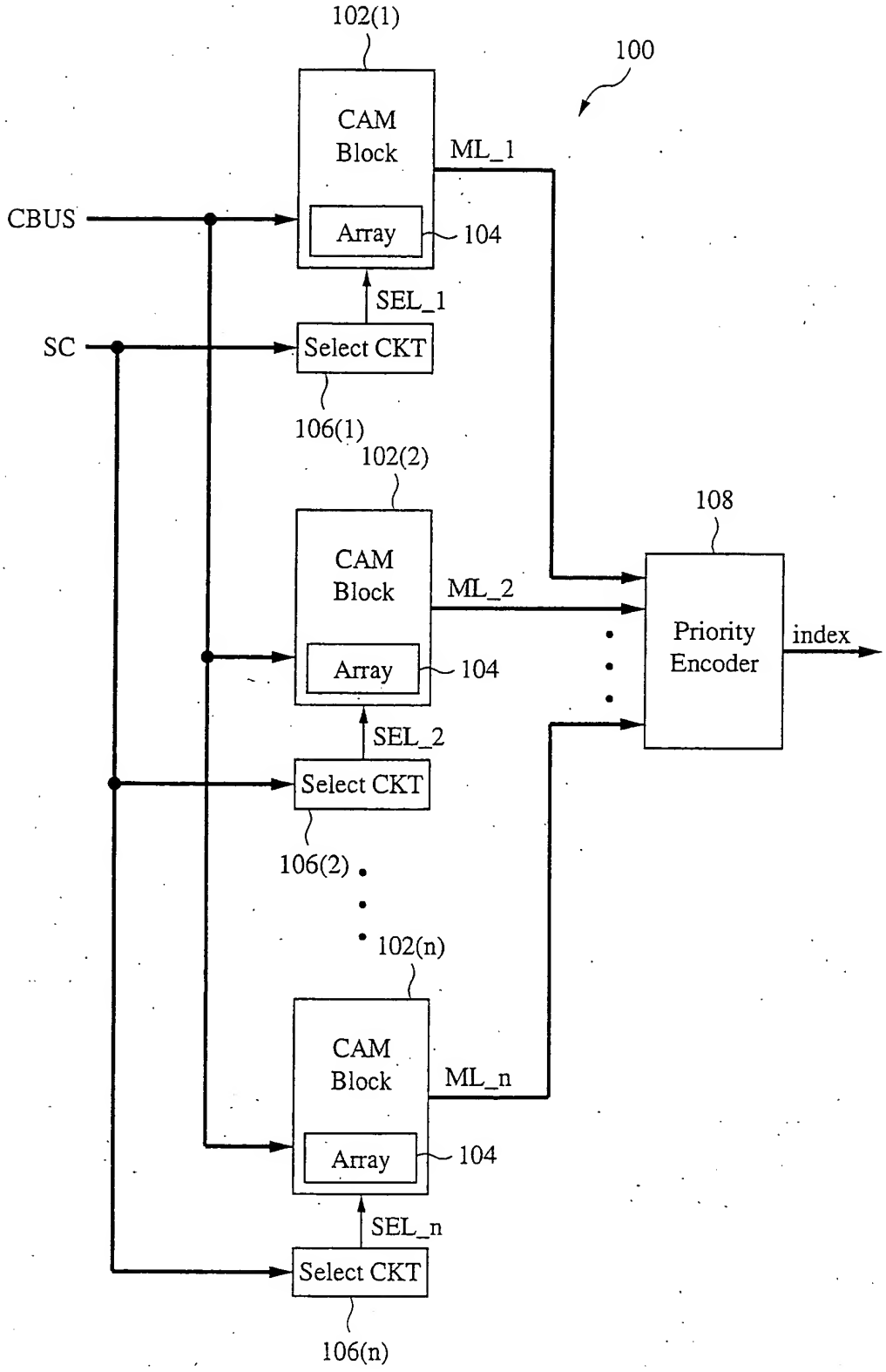

102(1)
100
CAM Block
ML_1
CBUS
Array
104
SEL_1
SC
Select CKT
106(1)
102(2)
108
CAM Block
ML_2
Priority Encoder
index
Array
104
SEL_2
Select CKT
106(2)
102(n)
CAM Block
ML_n
Array
104
SEL_n
Select CKT
106(n)

FIG. 1

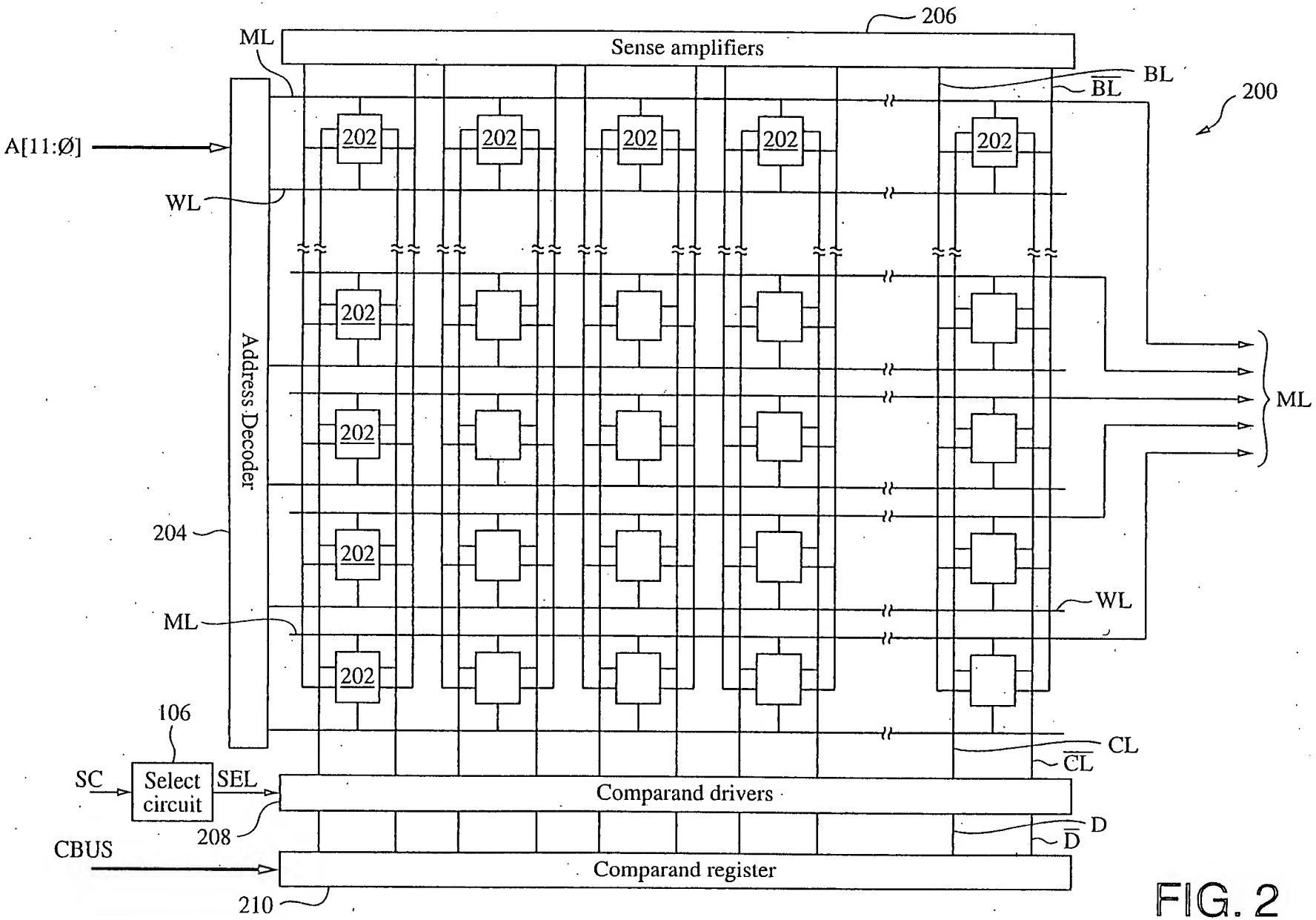

206
Sense amplifiers
ML
BL
$\overline{BL}$
200
A[11:Ø]
WL
202
Address Decoder
204
ML
106
SC
Select circuit
SEL
208
CBUS
Comparand drivers
Comparand register
210
CL
$\overline{CL}$
D
$\overline{D}$

FIG. 2

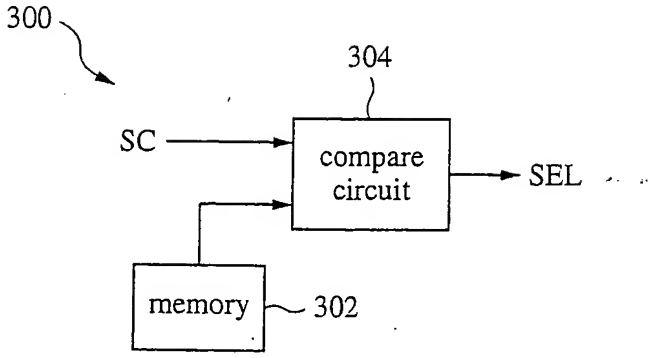

300
304
SC
compare circuit
SEL
memory
302

FIG. 3

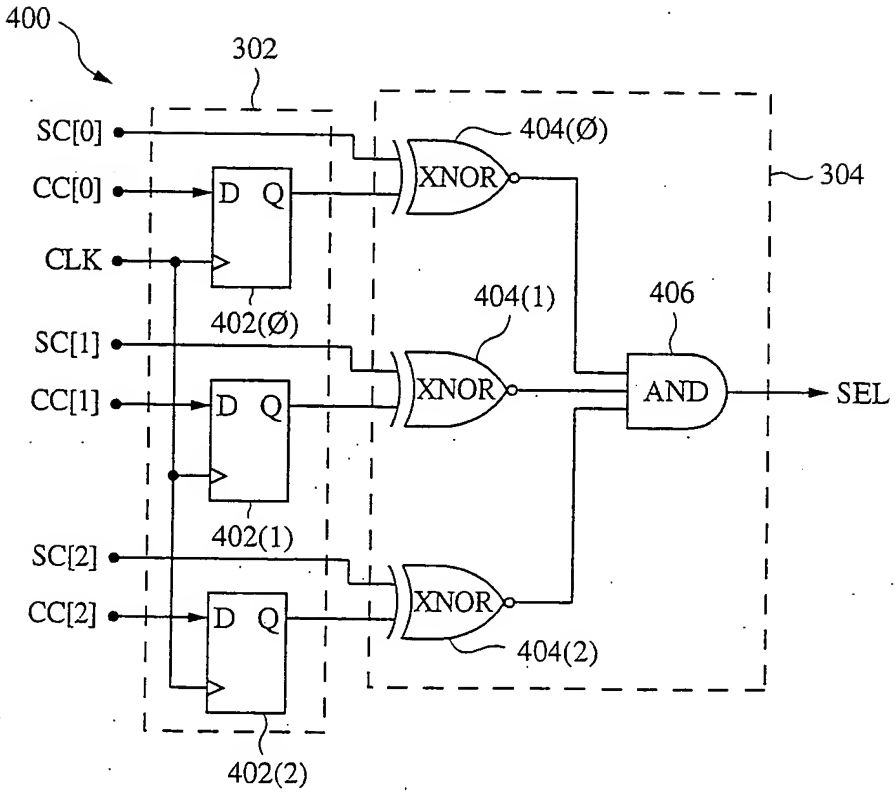

400
302
SC[0]
CC[0]
CLK
SC[1]
CC[1]
SC[2]
CC[2]
D Q
402(Ø)
402(1)
402(2)
XNOR
404(Ø)
404(1)
404(2)
AND
406
304
SEL

FIG. 4

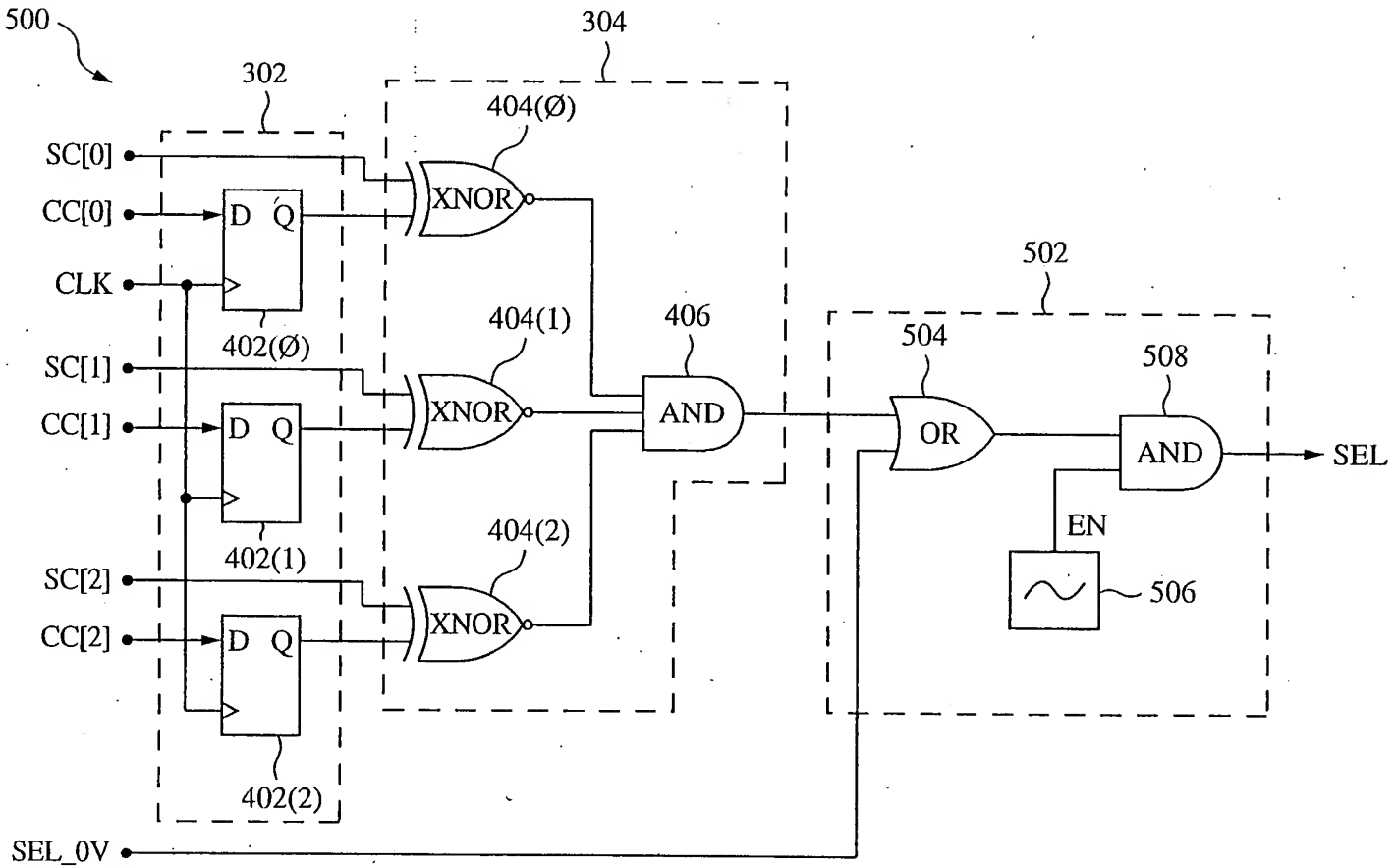

500
304
302
404(Ø)
SC[0]
CC[0]
D Q
XNOR
CLK
502
404(1)
406
504
508
402(Ø)
SC[1]
CC[1]
D Q
XNOR
AND
OR
AND
SEL
404(2)
EN
402(1)
SC[2]
CC[2]
D Q
XNOR
506
402(2)
SEL_0V

FIG. 5

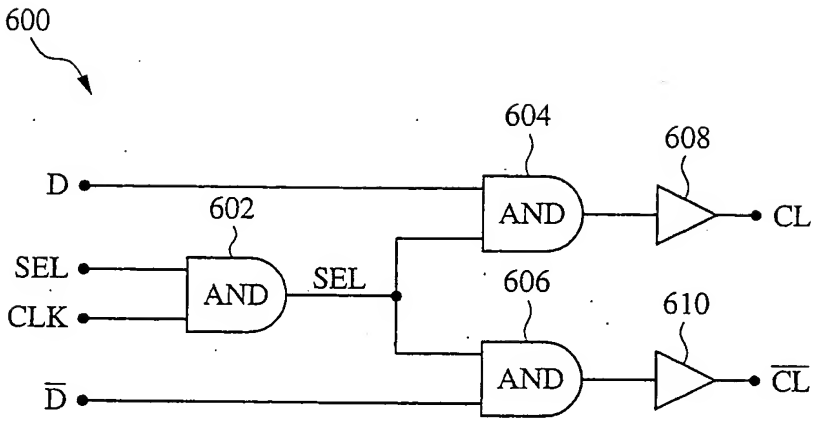

600
604
608
D
602
AND
CL
SEL
AND
SEL
606
610
CLK
AND
$\overline{D}$
$\overline{CL}$

FIG. 6

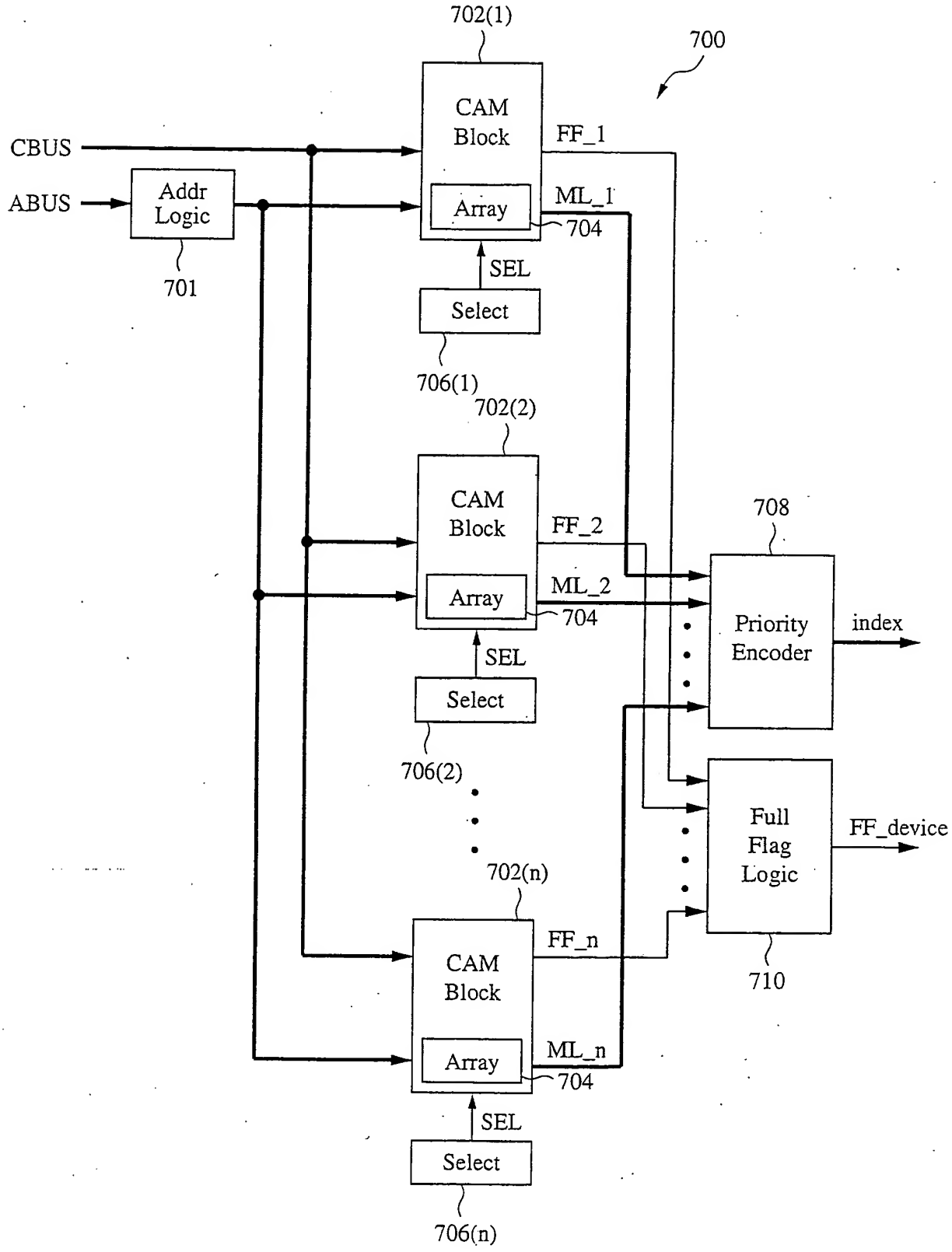

702(1)
700
CAM Block
FF_1
CBUS
ABUS
Addr Logic
Array
ML_1
704
SEL
Select
701
706(1)
702(2)
CAM Block
FF_2
708
Array
ML_2
704
Priority Encoder
index
SEL
Select
706(2)
Full Flag Logic
FF_device
702(n)
CAM Block
FF_n
Array
ML_n
704
710
SEL
Select
706(n)

FIG. 7

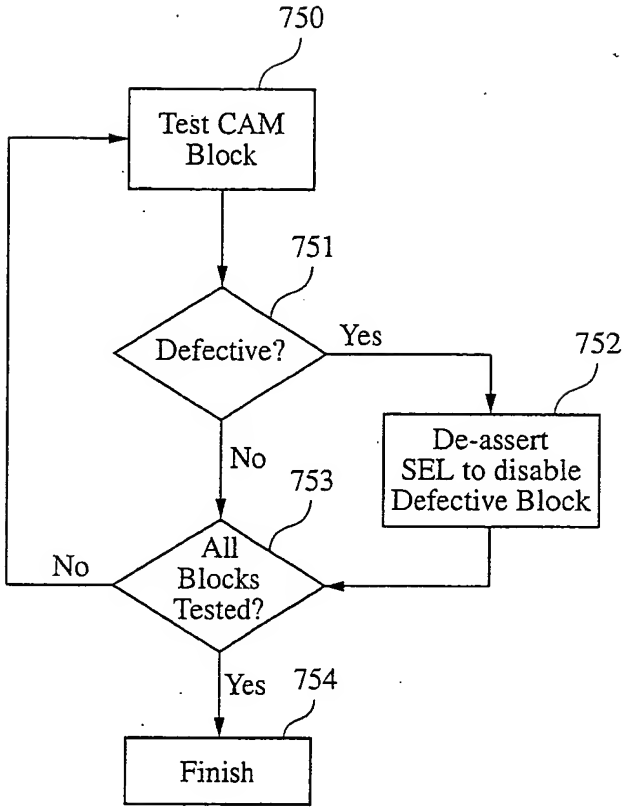

750
Test CAM Block
751
Defective?
Yes
752
De-assert SEL to disable Defective Block
No
753
All Blocks Tested?
No
Yes
754
Finish

FIG. 8

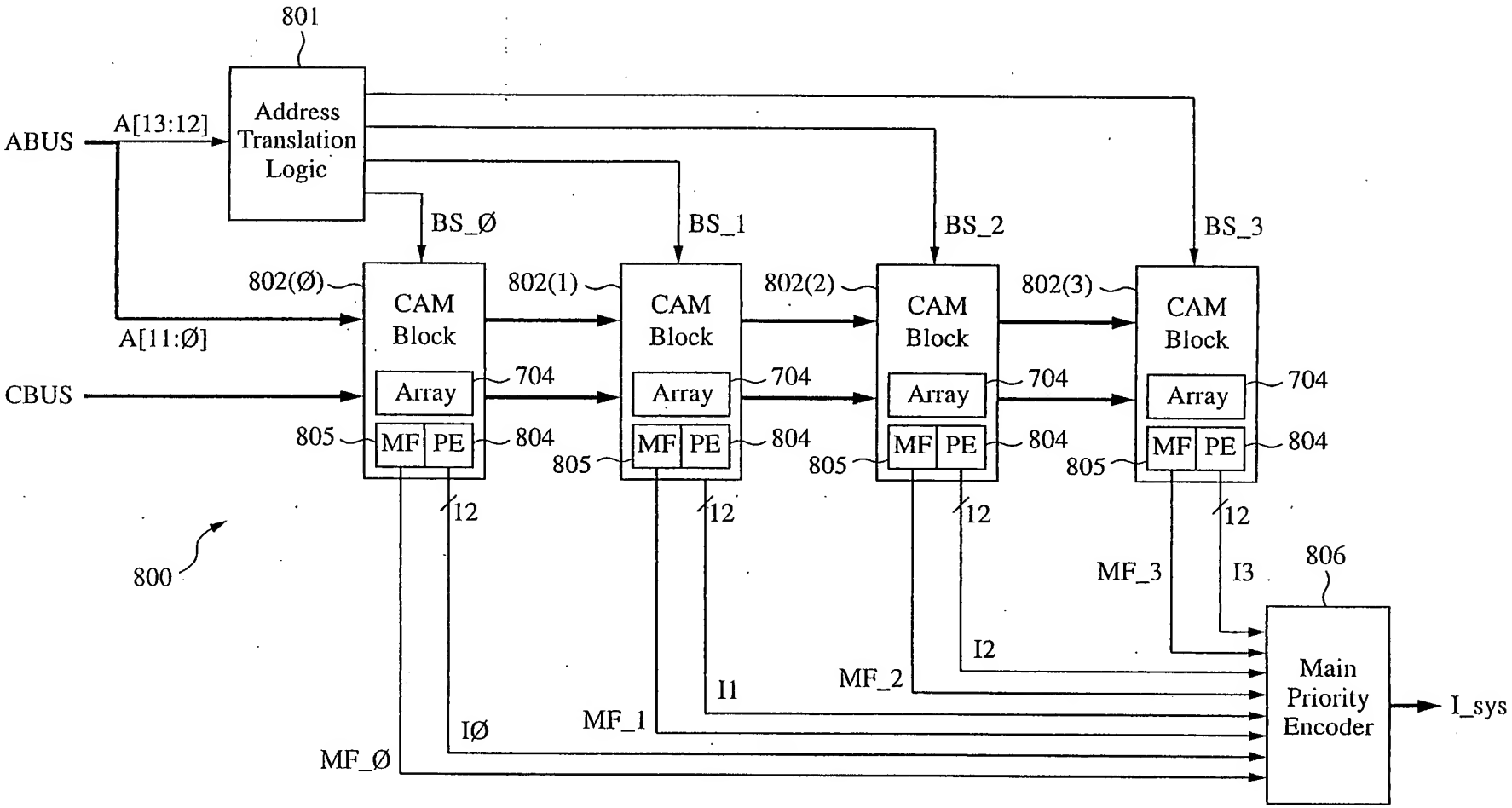

801
Address Translation Logic
ABUS
A[13:12]
A[11:Ø]
CBUS
BS_Ø
BS_1
BS_2
BS_3
802(Ø)
802(1)
802(2)
802(3)
CAM Block
Array
MF
PE
704
804
805
12
800
MF_3
I3
806
I2
MF_2
I1
MF_1
IØ
MF_Ø
Main Priority Encoder
I_sys

FIG. 9

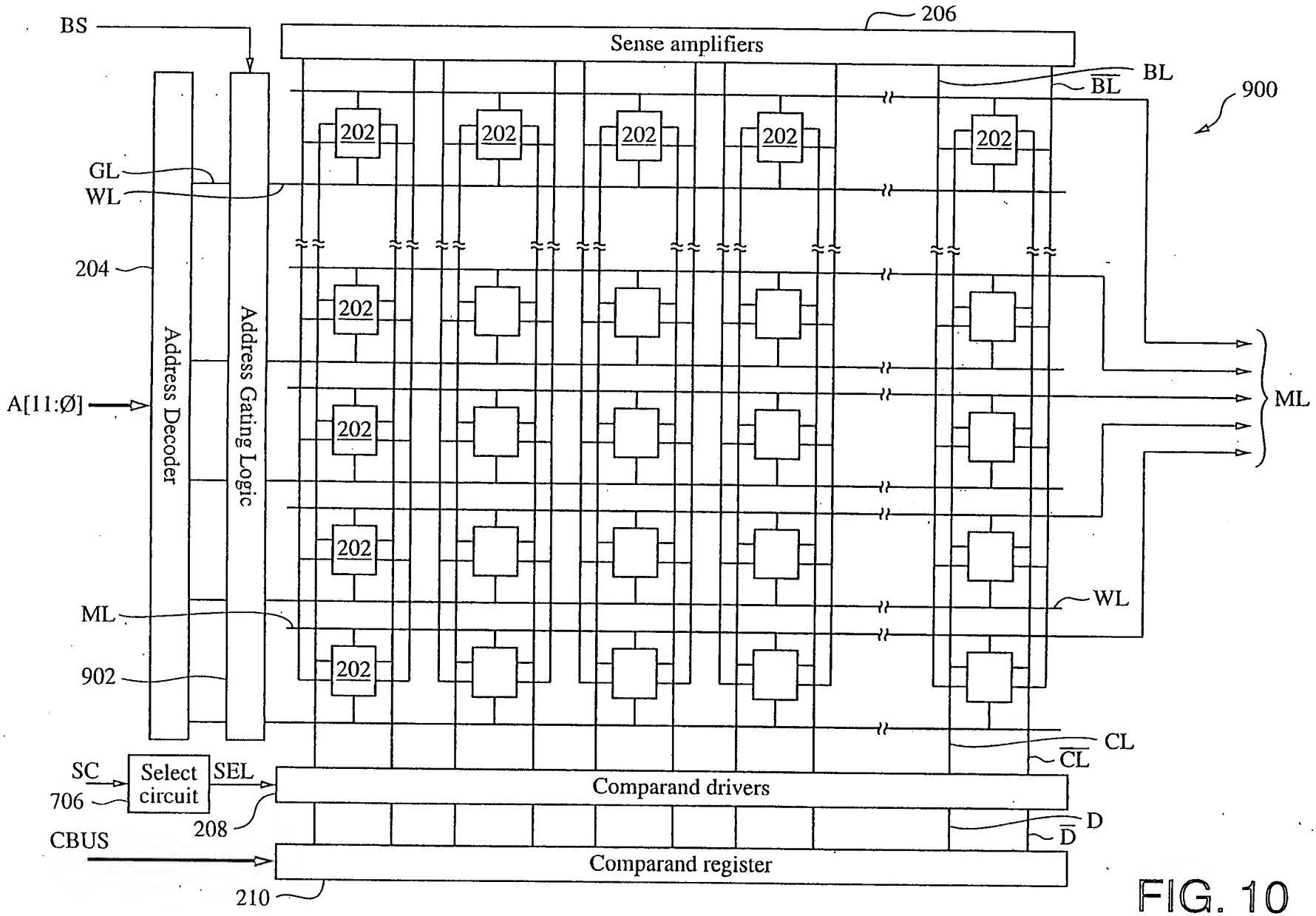

BS
206
Sense amplifiers
BL
$\overline{BL}$
900
202
GL
WL
204
Address Decoder
Address Gating Logic
A[11:Ø]
ML
902
WL
CL
$\overline{CL}$
SC
Select circuit
SEL
706
208
Comparand drivers
D
$\overline{D}$
CBUS
Comparand register
210

FIG. 10

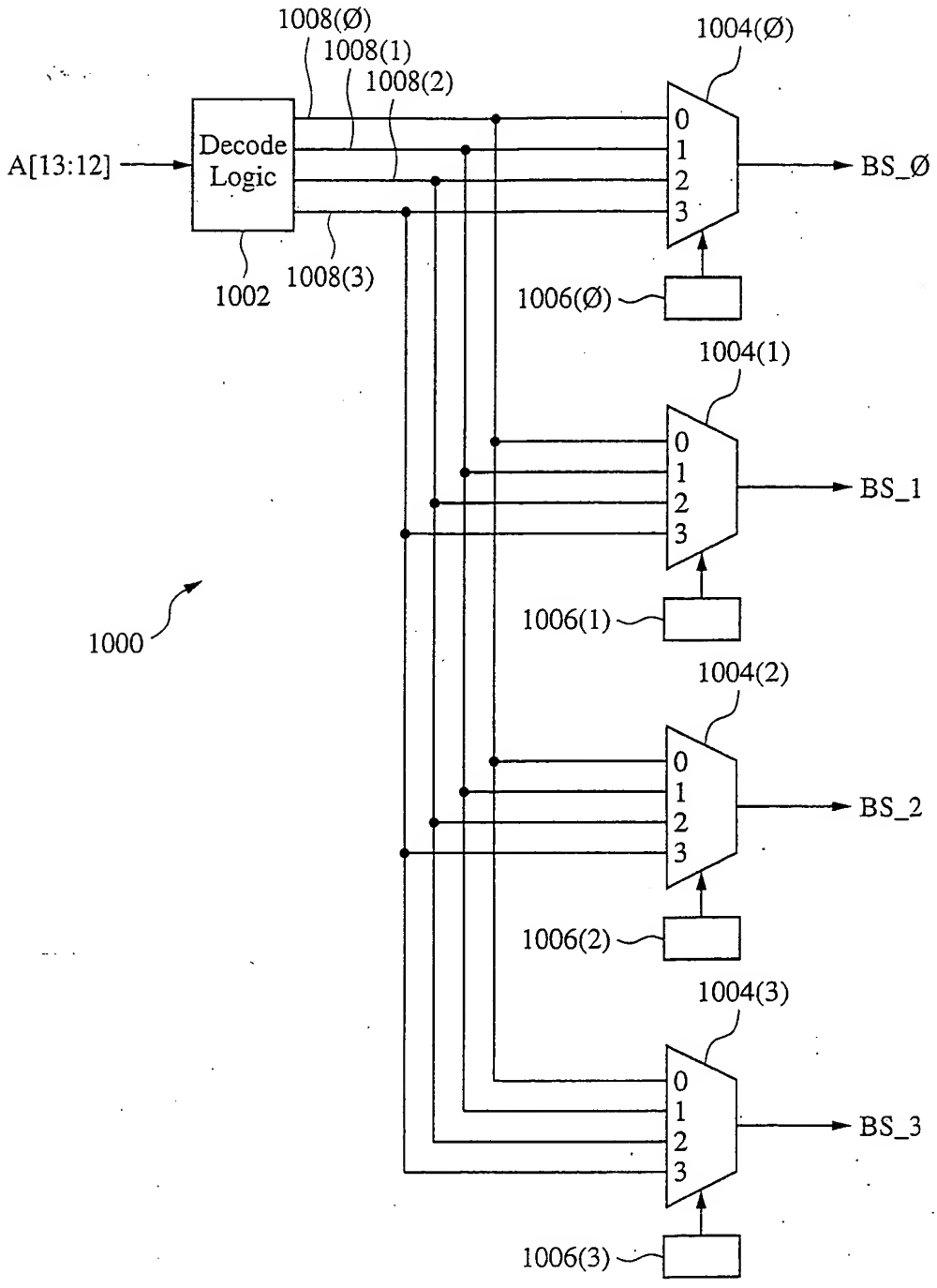

1008(Ø)
1008(1)
1008(2)
1004(Ø)
A[13:12]
Decode Logic
0
1
2
3
BS_Ø
1002
1008(3)
1006(Ø)
1004(1)
BS_1
1000
1006(1)
1004(2)
BS_2
1006(2)
1004(3)
BS_3
1006(3)

FIG. 11

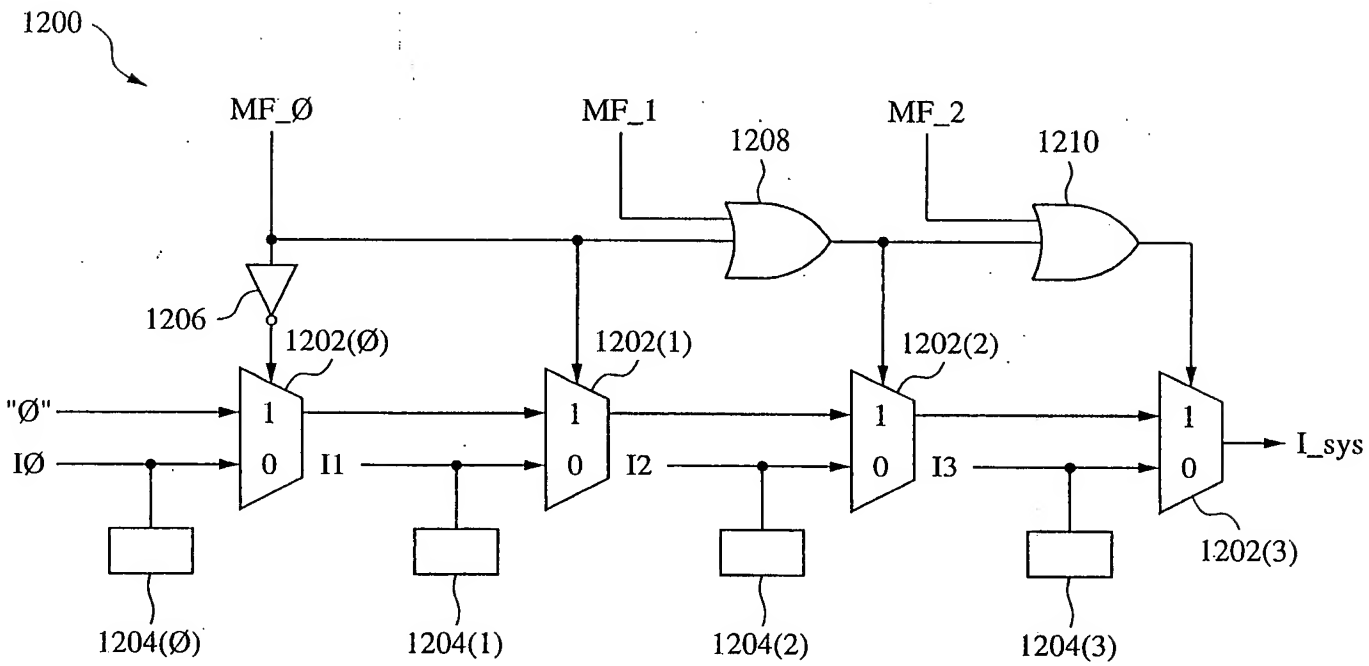

1200
MF_Ø
MF_1
MF_2
1208
1210
1206
1202(Ø)
1202(1)
1202(2)
"Ø"
IØ
1
0
I1
I2
I3
I_sys
1202(3)
1204(Ø)
1204(1)
1204(2)
1204(3)

FIG. 12

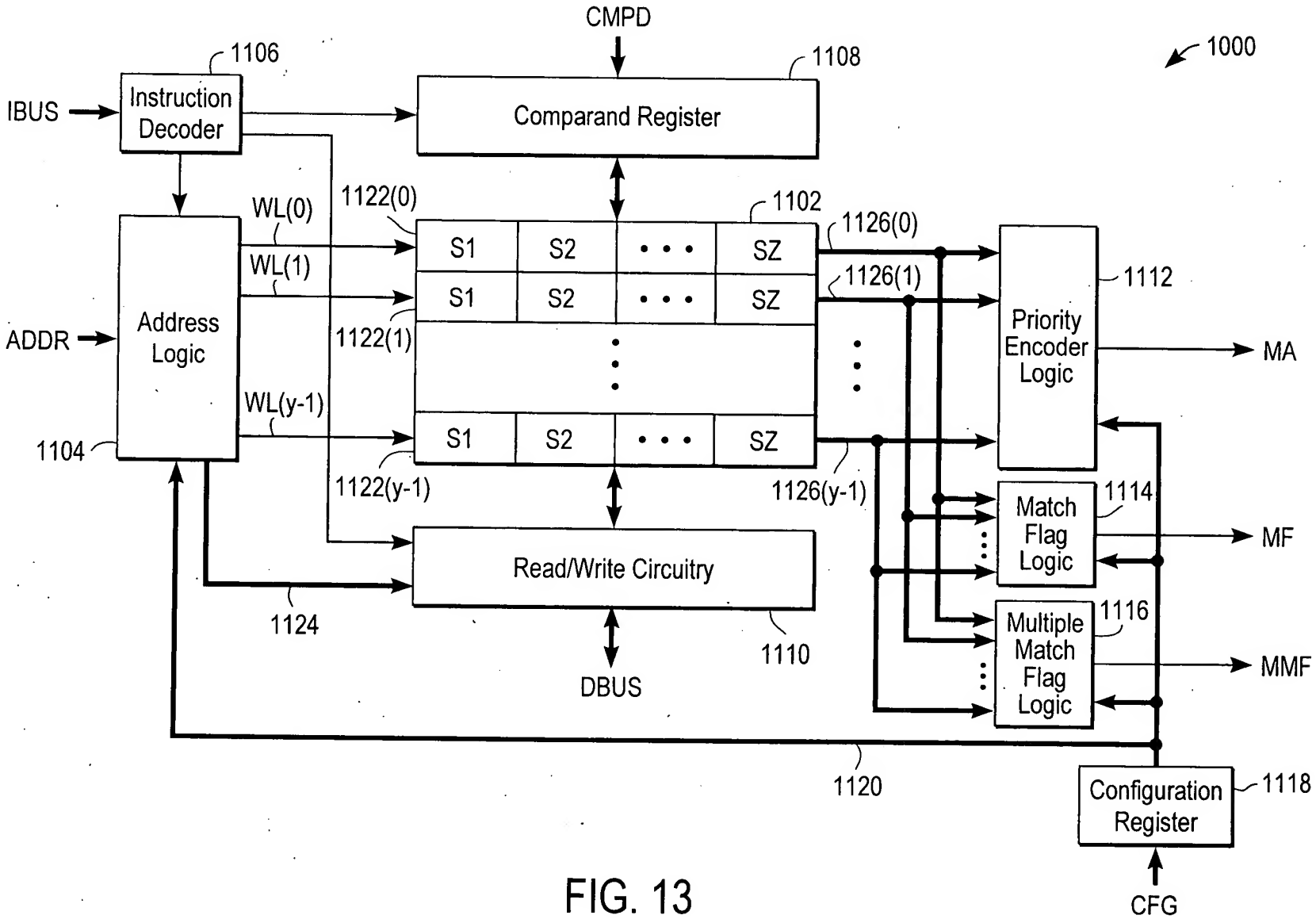

CMPD
1000
1106
1108
IBUS
Instruction Decoder
Comparand Register
1102
1122(0)
WL(0)
WL(1)
1126(0)
1126(1)
S1
S2
SZ
ADDR
Address Logic
1122(1)
1112
Priority Encoder Logic
MA
WL(y-1)
1104
1122(y-1)
1126(y-1)
1114
Match Flag Logic
MF
Read/Write Circuitry
1124
1110
1116
Multiple Match Flag Logic
MMF
DBUS
1120
Configuration Register
1118
CFG

FIG. 13

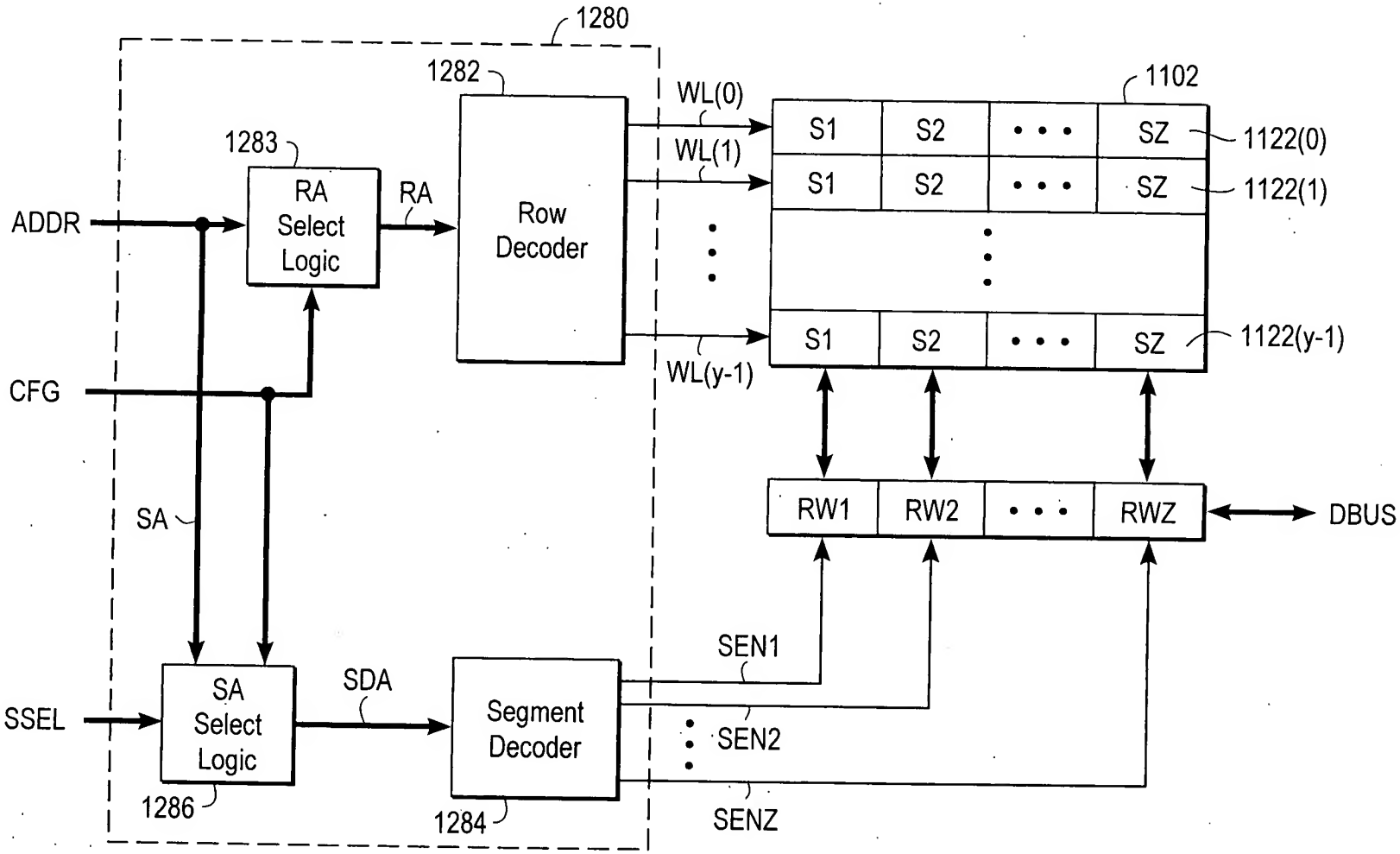

1280
1282
1283
RA Select Logic
RA
Row Decoder
ADDR
CFG
SA
SSEL
SA Select Logic
SDA
Segment Decoder
1286
1284
WL(0)
WL(1)
WL(y-1)
1102
S1
S2
SZ
1122(0)
1122(1)
1122(y-1)
RW1
RW2
RWZ
DBUS
SEN1
SEN2
SENZ

FIG. 14

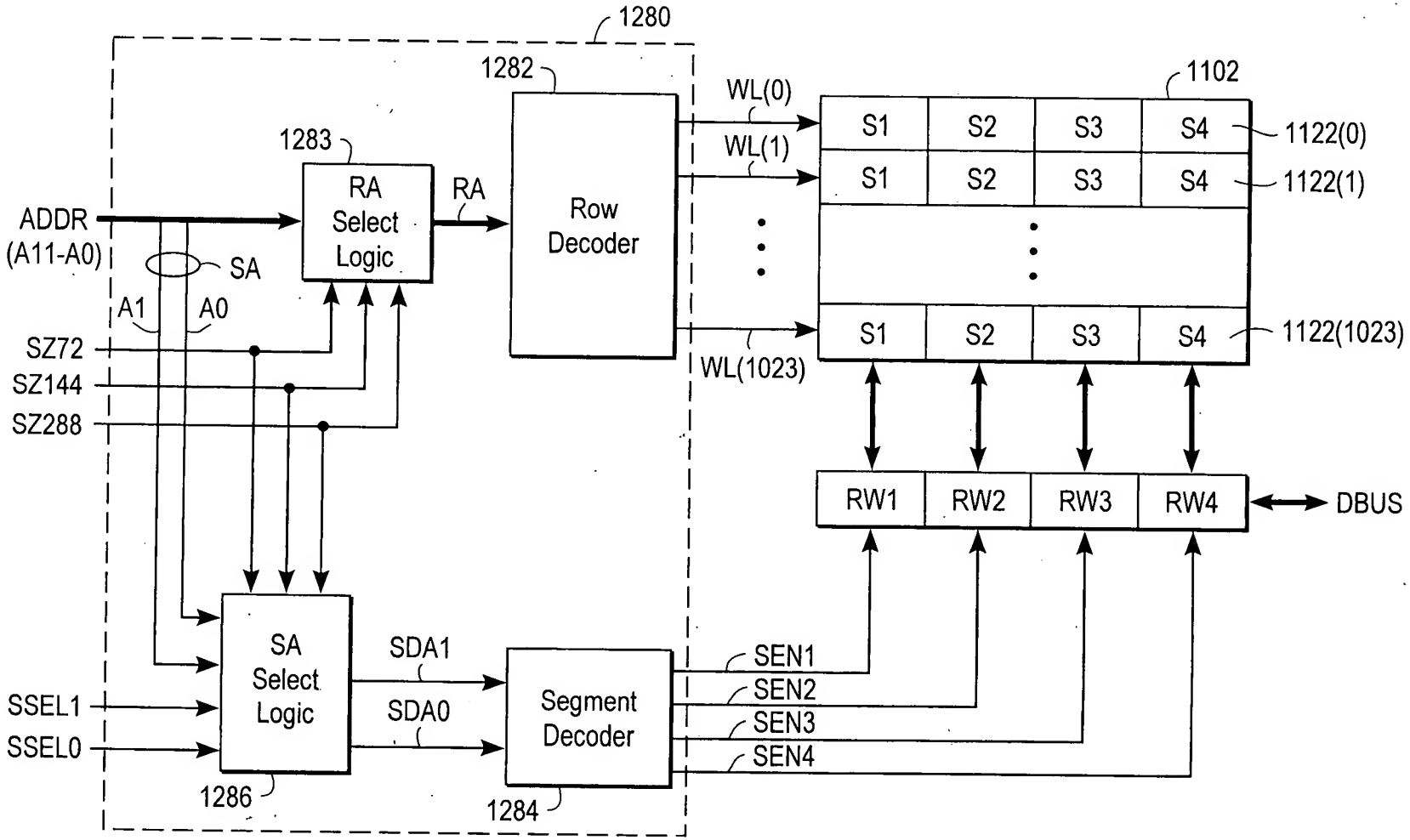

1280
1282
1283
1102
RA
Select
Logic
RA
Row
Decoder
WL(0)
WL(1)
WL(1023)
ADDR
(A11-A0)
SA
A1
A0
SZ72
SZ144
SZ288
S1
S2
S3
S4
1122(0)
1122(1)
1122(1023)
RW1
RW2
RW3
RW4
DBUS
SA
Select
Logic
SDA1
SDA0
SSEL1
SSEL0
Segment
Decoder
SEN1
SEN2
SEN3
SEN4
1286
1284

FIG. 15

CONFIG	CONFIG SIGNAL	ADDR	RA	SA	SDA
4K x 72	SZ1	A11-A0	A11-A2	A1-A0	A1-A0
2K x 144	SZG1	A10-A0	A10-A1	A0	A0, SSEL0
1K x 288	SZGZ	A9-A0	A9-A0	—	SSEL1-SSEL0

FIG. 16

CONFIG	A1	A0	SSEL1	SSEL0	SEN4	SEN3	SEN2	SEN1
4k x 72	0	0	X	X	0	0	0	1
4k x 72	0	1	X	X	0	0	1	0
4k x 72	1	0	X	X	0	1	0	0
4k x 72	1	1	X	X	1	0	0	0
2k x 144	X	0	X	0	0	0	0	1
2k x 144	X	0	X	1	0	0	1	0
2k x 144	X	1	X	0	0	1	0	0
2k x 144	X	1	X	1	1	0	0	0
1k x 288	X	X	0	0	0	0	0	1
1k x 288	X	X	0	1	0	0	1	0
1k x 288	X	X	1	0	0	1	0	0
1k x 288	X	X	1	1	1	0	0	0

FIG. 17

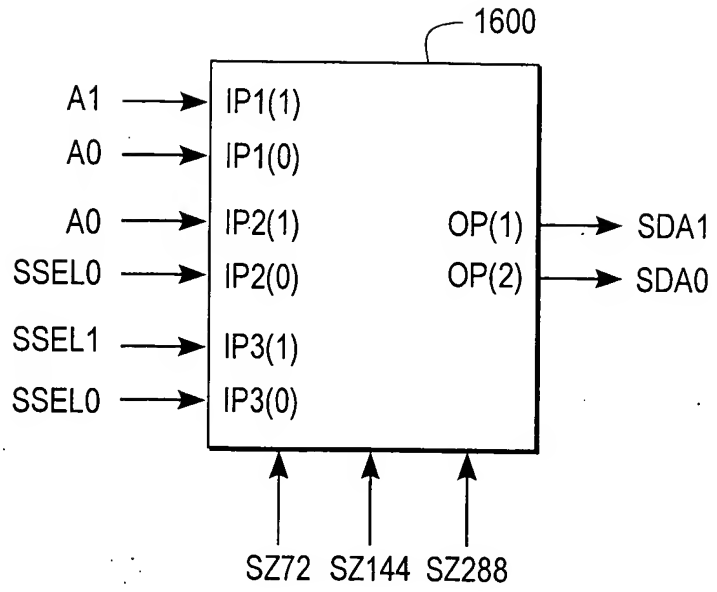


FIG. 18A

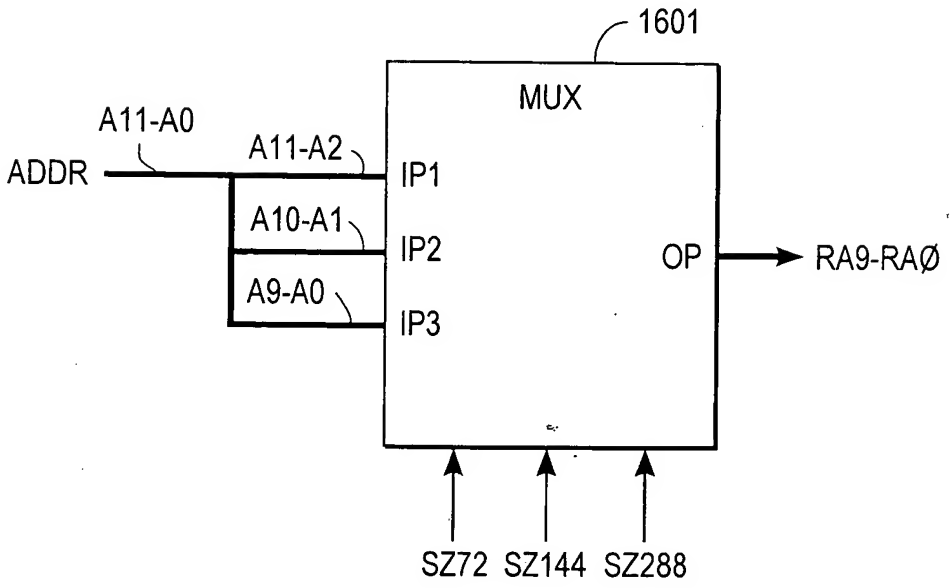


FIG. 18B

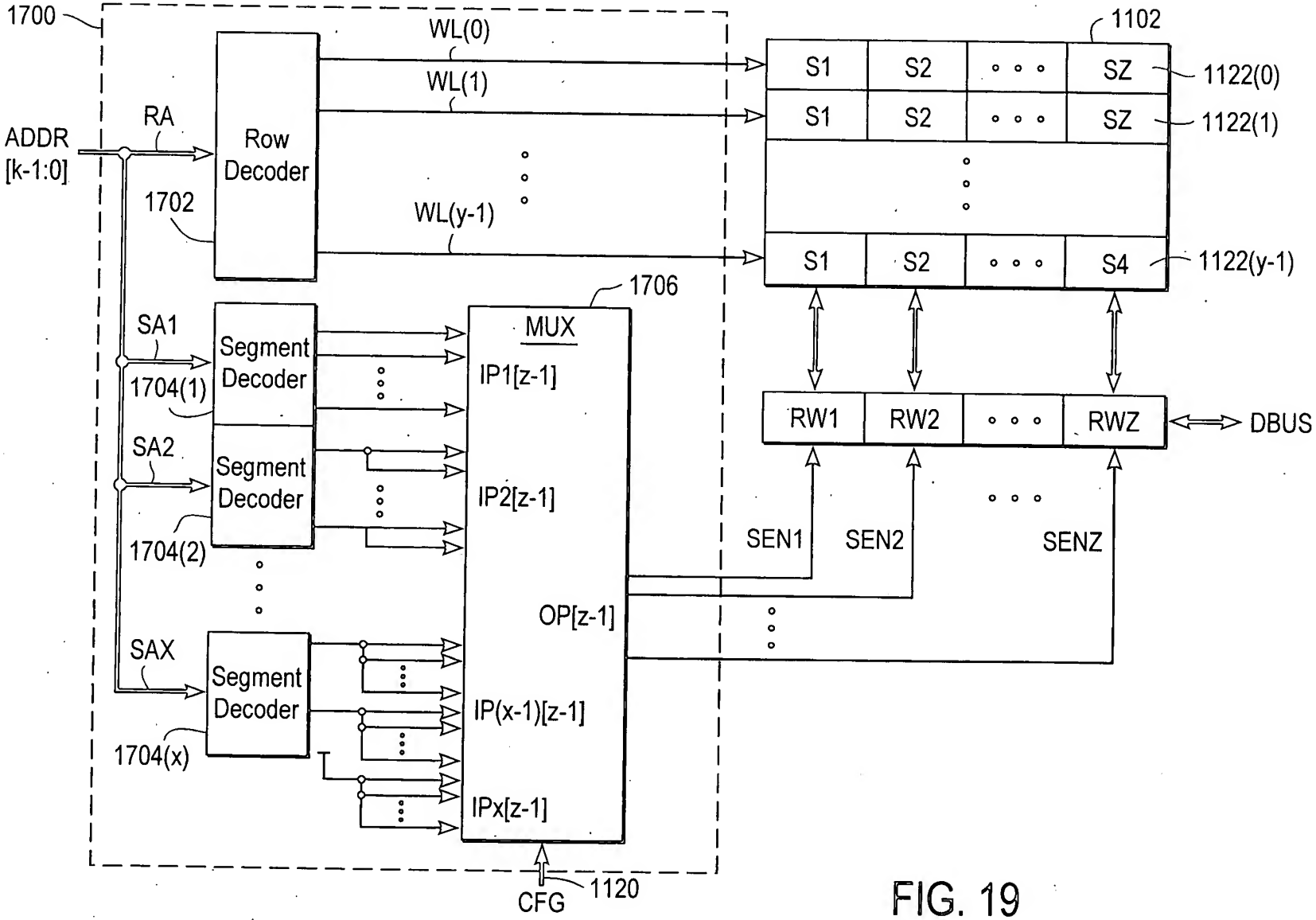

1700
1102
WL(0)
WL(1)
WL(y-1)
ADDR
[k-1:0]
RA
Row
Decoder
1702
S1
S2
SZ
1122(0)
1122(1)
S4
1122(y-1)
1706
MUX
SA1
Segment
Decoder
1704(1)
SA2
1704(2)
SAX
1704(x)
IP1[z-1]
IP2[z-1]
IP(x-1)[z-1]
IPx[z-1]
OP[z-1]
RW1
RW2
RWZ
DBUS
SEN1
SEN2
SENZ
CFG
1120

FIG. 19

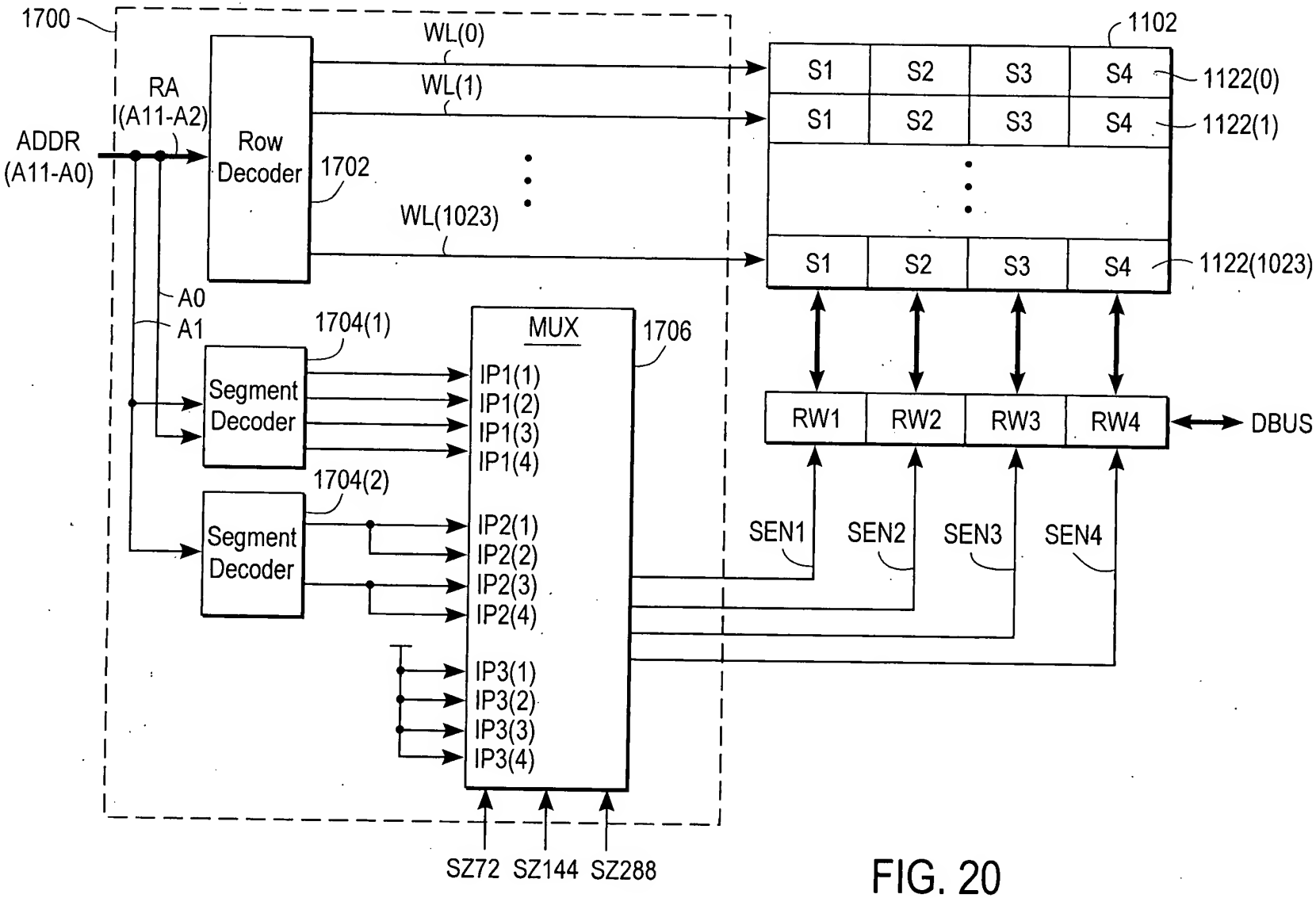

1700
WL(0)
WL(1)
WL(1023)
RA
(A11-A2)
ADDR
(A11-A0)
Row
Decoder
1702
A0
A1
1704(1)
Segment
Decoder
1704(2)
Segment
Decoder
MUX
1706
IP1(1)
IP1(2)
IP1(3)
IP1(4)
IP2(1)
IP2(2)
IP2(3)
IP2(4)
IP3(1)
IP3(2)
IP3(3)
IP3(4)
SZ72
SZ144
SZ288
1102
S1
S2
S3
S4
1122(0)
1122(1)
1122(1023)
RW1
RW2
RW3
RW4
DBUS
SEN1
SEN2
SEN3
SEN4

FIG. 20

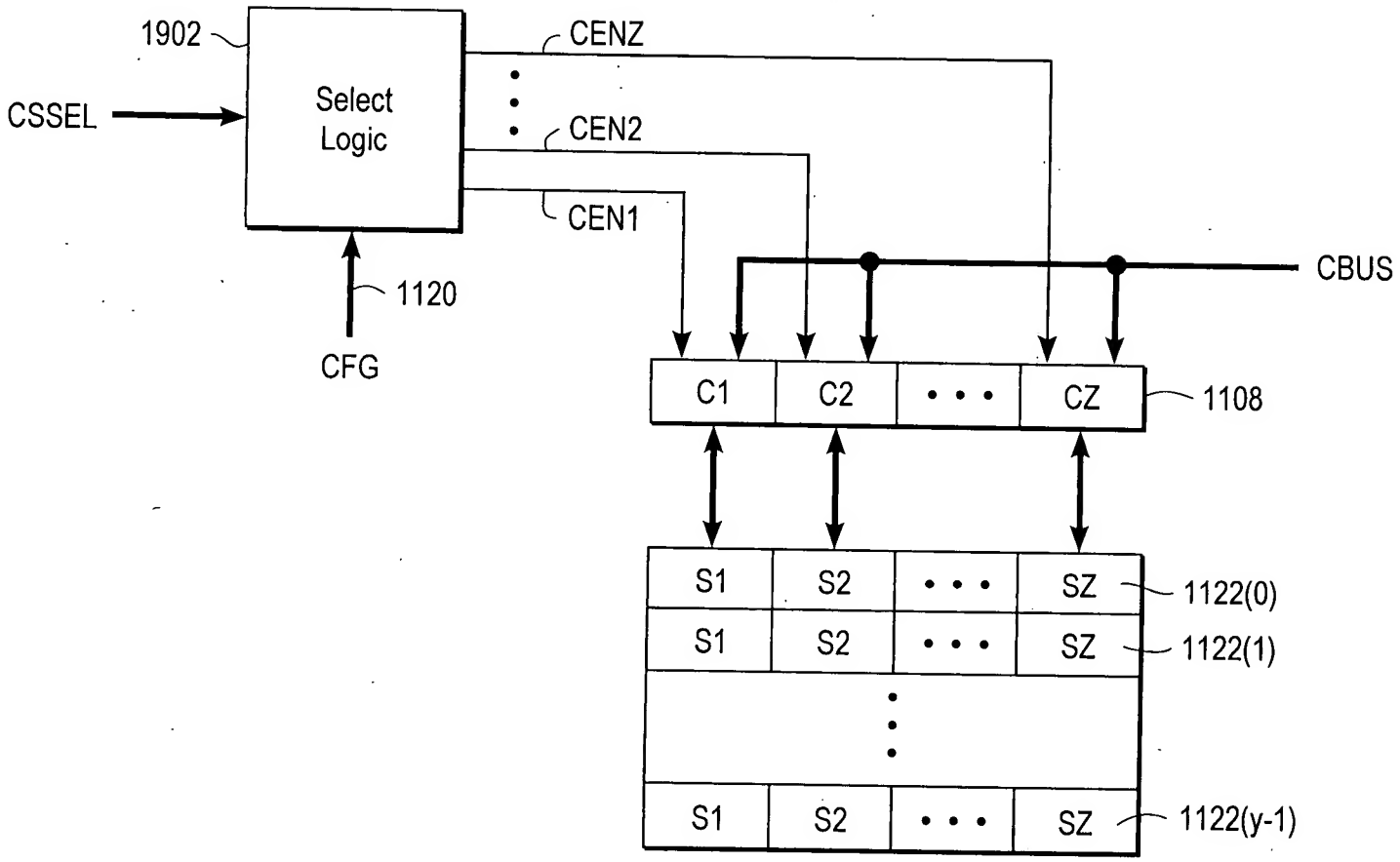

1902
Select Logic
CSSEL
CENZ
CEN2
CEN1
1120
CFG
CBUS
C1
C2
CZ
1108
S1
S2
SZ
1122(0)
1122(1)
1122(y-1)

FIG. 21

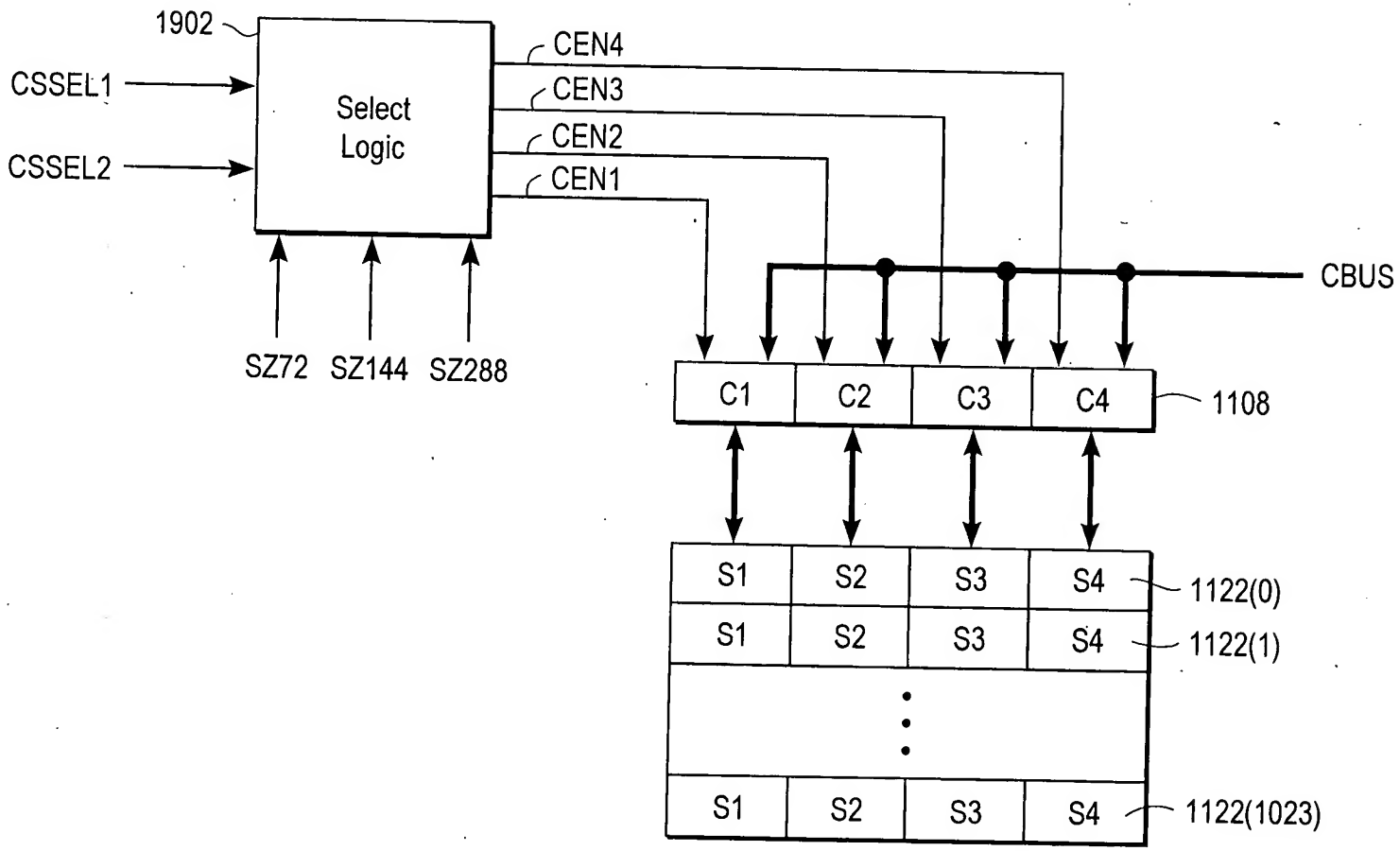

1902
CSSEL1
CSSEL2
Select Logic
CEN4
CEN3
CEN2
CEN1
SZ72
SZ144
SZ288
CBUS
C1
C2
C3
C4
1108
S1
S2
S3
S4
1122(0)
1122(1)
1122(1023)

FIG. 22

CONFIG	CSSEL1	CSSEL0	CEN1	CEN2	CEN3	CEN4
4k x 72	X	X	1	1	1	1
2k x 144	X	0	1	0	1	0
2k x 144	X	1	0	1	0	1
1k x 288	0	0	1	0	0	0
1k x 288	0	1	0	1	0	0
1k x 288	1	0	0	0	1	0
1k x 288	1	1	0	0	0	1

FIG. 23

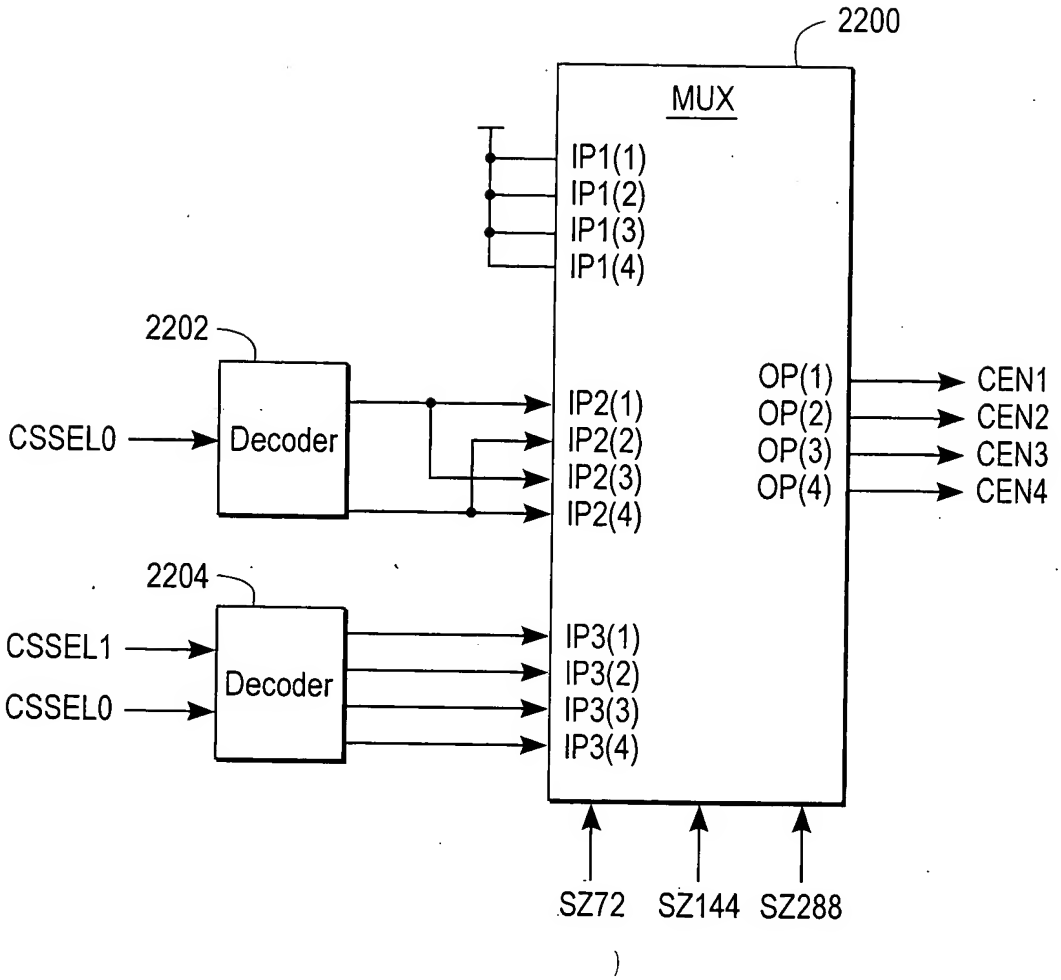

2200
MUX
IP1(1)
IP1(2)
IP1(3)
IP1(4)
2202
CSSEL0
Decoder
IP2(1)
IP2(2)
IP2(3)
IP2(4)
OP(1)
OP(2)
OP(3)
OP(4)
CEN1
CEN2
CEN3
CEN4
2204
CSSEL1
CSSEL0
Decoder
IP3(1)
IP3(2)
IP3(3)
IP3(4)
SZ72
SZ144
SZ288

FIG. 24

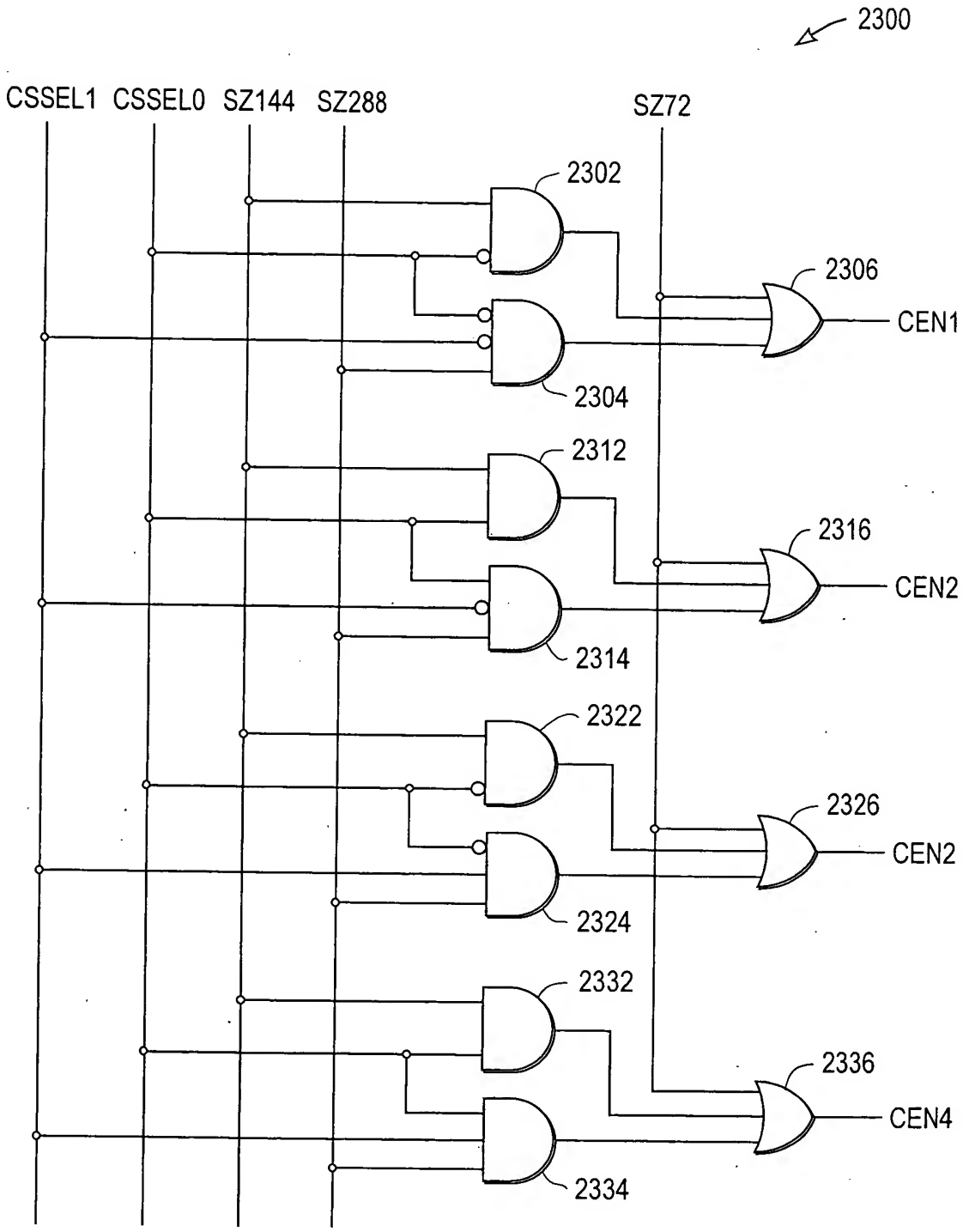

2300
CSSEL1
CSSEL0
SZ144
SZ288
SZ72
2302
2306
CEN1
2304
2312
2316
CEN2
2314
2322
2326
CEN2
2324
2332
2336
CEN4
2334

FIG. 25

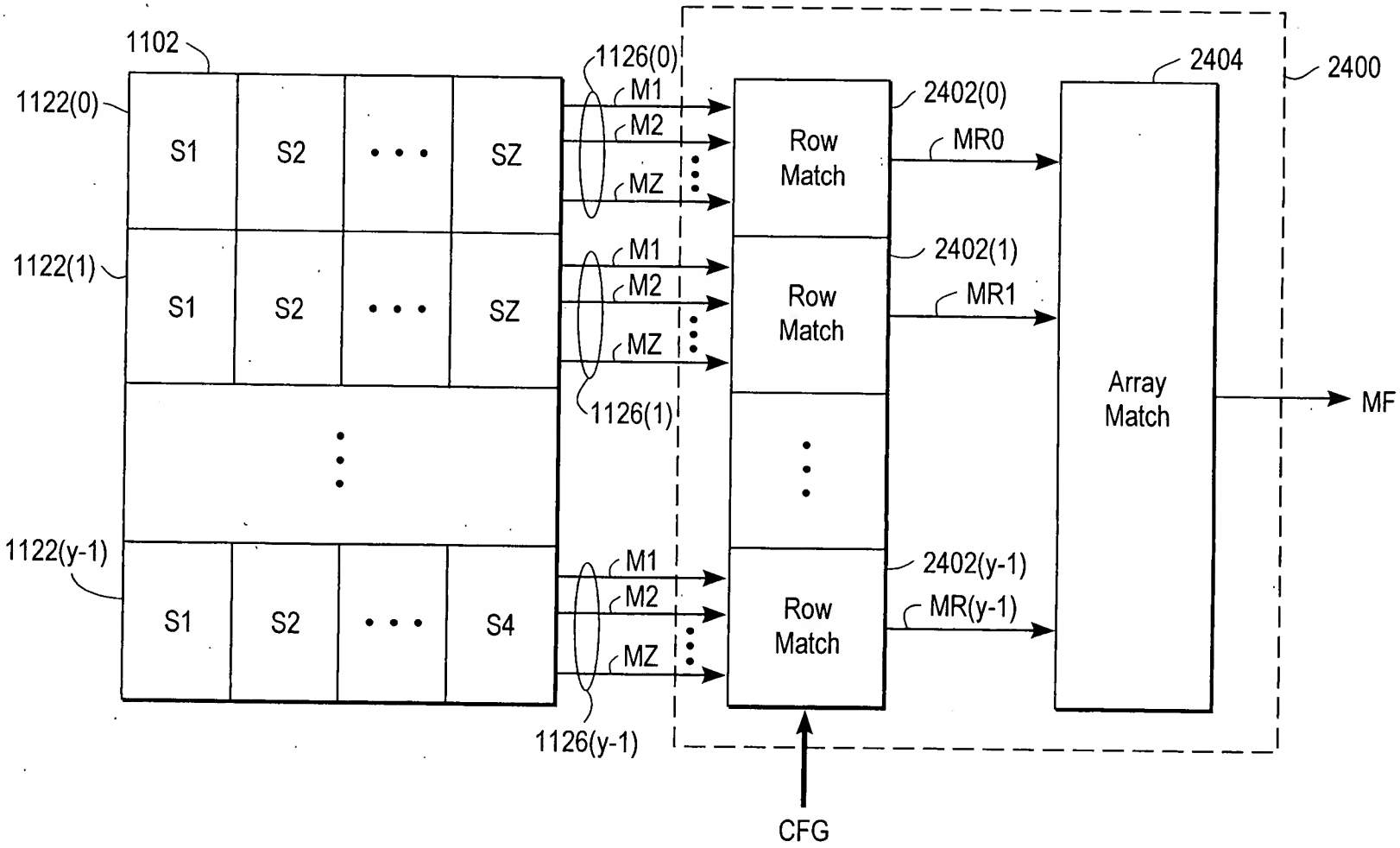

1102
1122(0)
1122(1)
1122(y-1)
S1
S2
S4
SZ
1126(0)
1126(1)
1126(y-1)
M1
M2
MZ
Row Match
2402(0)
2402(1)
2402(y-1)
MR0
MR1
MR(y-1)
2404
Array Match
2400
MF
CFG

FIG. 26

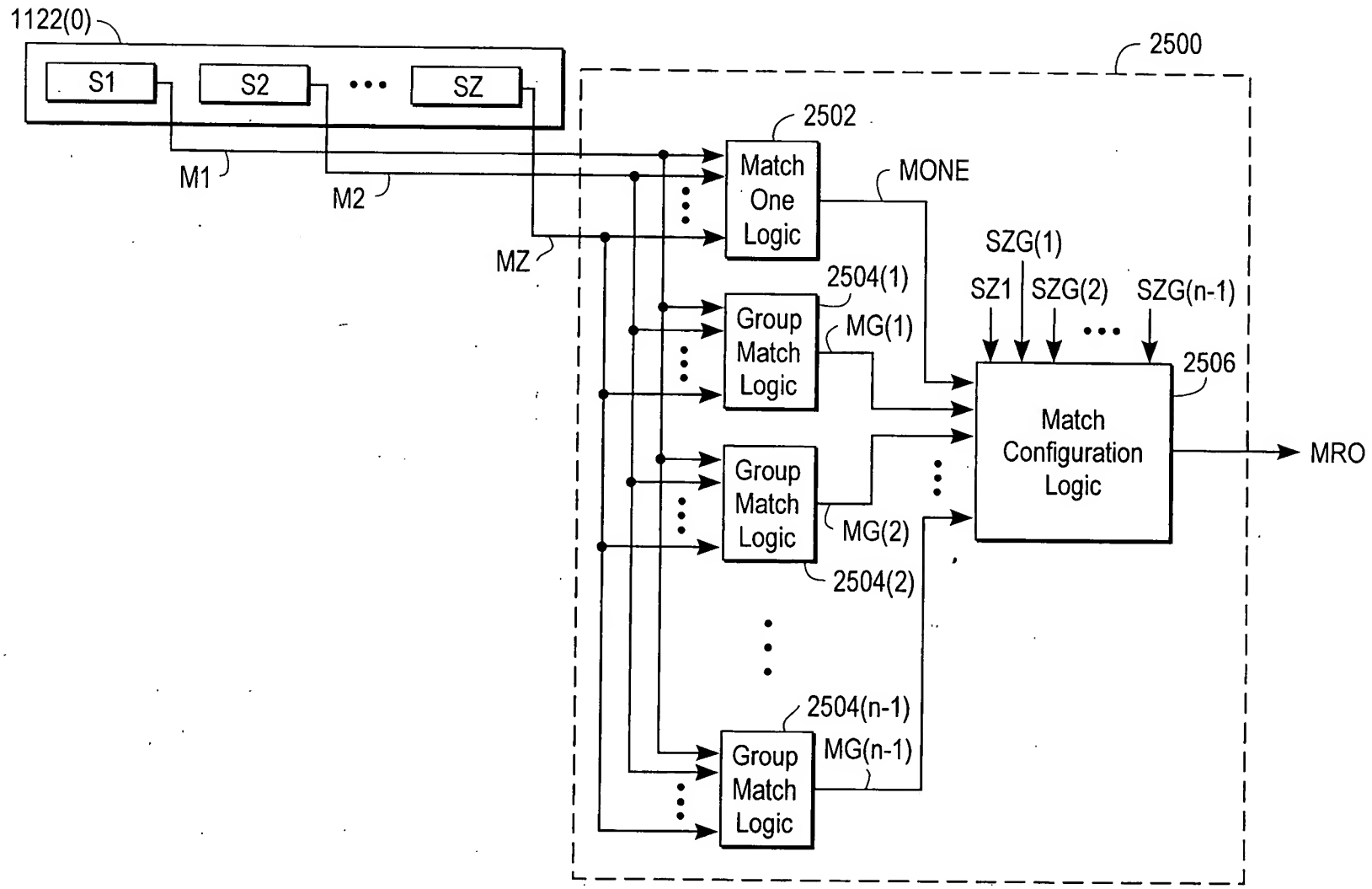

1122(0)
S1
S2
SZ
M1
M2
MZ
2500
2502
Match One Logic
MONE
SZG(1)
SZ1
SZG(2)
SZG(n-1)
2504(1)
Group Match Logic
MG(1)
2506
Match Configuration Logic
MRO
Group Match Logic
MG(2)
2504(2)
2504(n-1)
Group Match Logic
MG(n-1)

FIG. 27

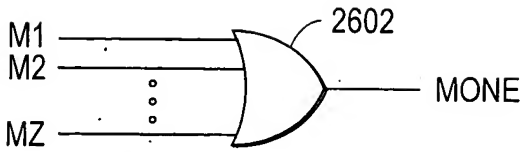


FIG. 28

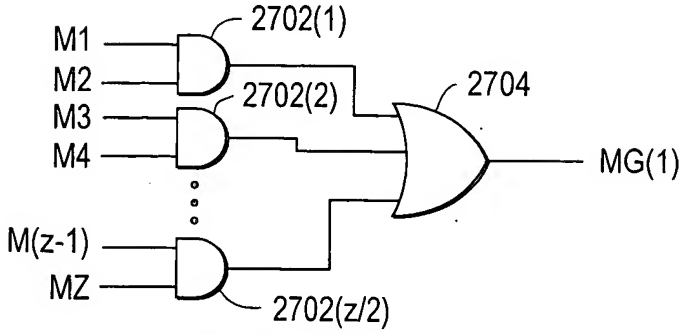


FIG. 29A

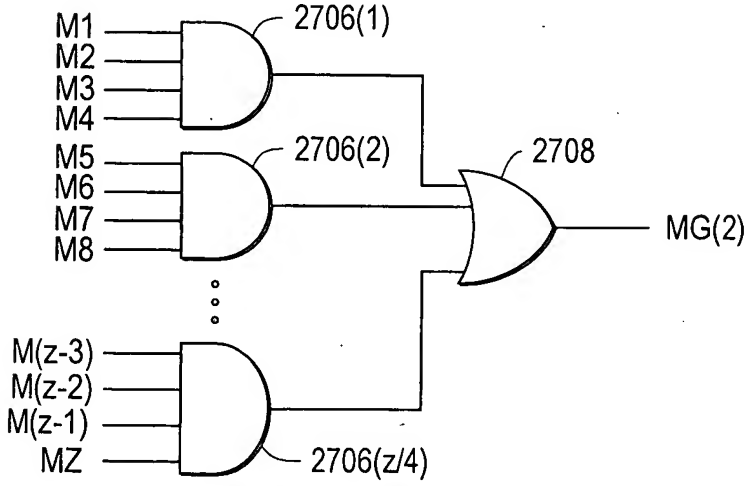


FIG. 29B

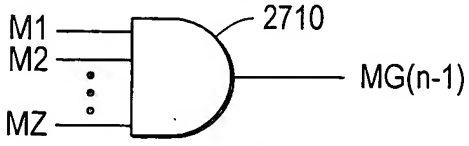


FIG. 29C

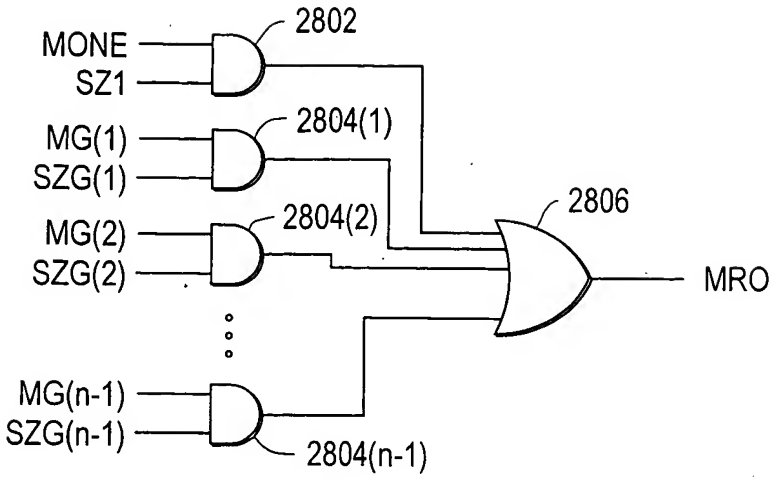

MONE
SZ1
2802
MG(1)
SZG(1)
2804(1)
MG(2)
SZG(2)
2804(2)
2806
MRO
MG(n-1)
SZG(n-1)
2804(n-1)

FIG. 30

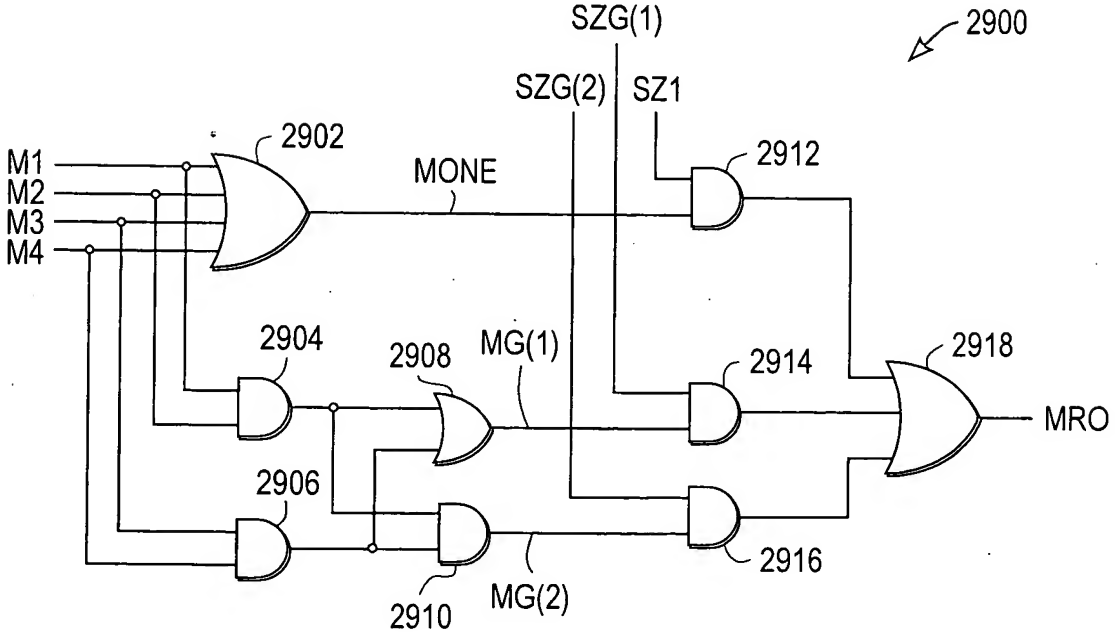

SZG(1)
2900
SZG(2)
SZ1
2902
M1
M2
M3
M4
MONE
2912
2904
2908
MG(1)
2914
2918
MRO
2906
2916
2910
MG(2)

FIG. 31

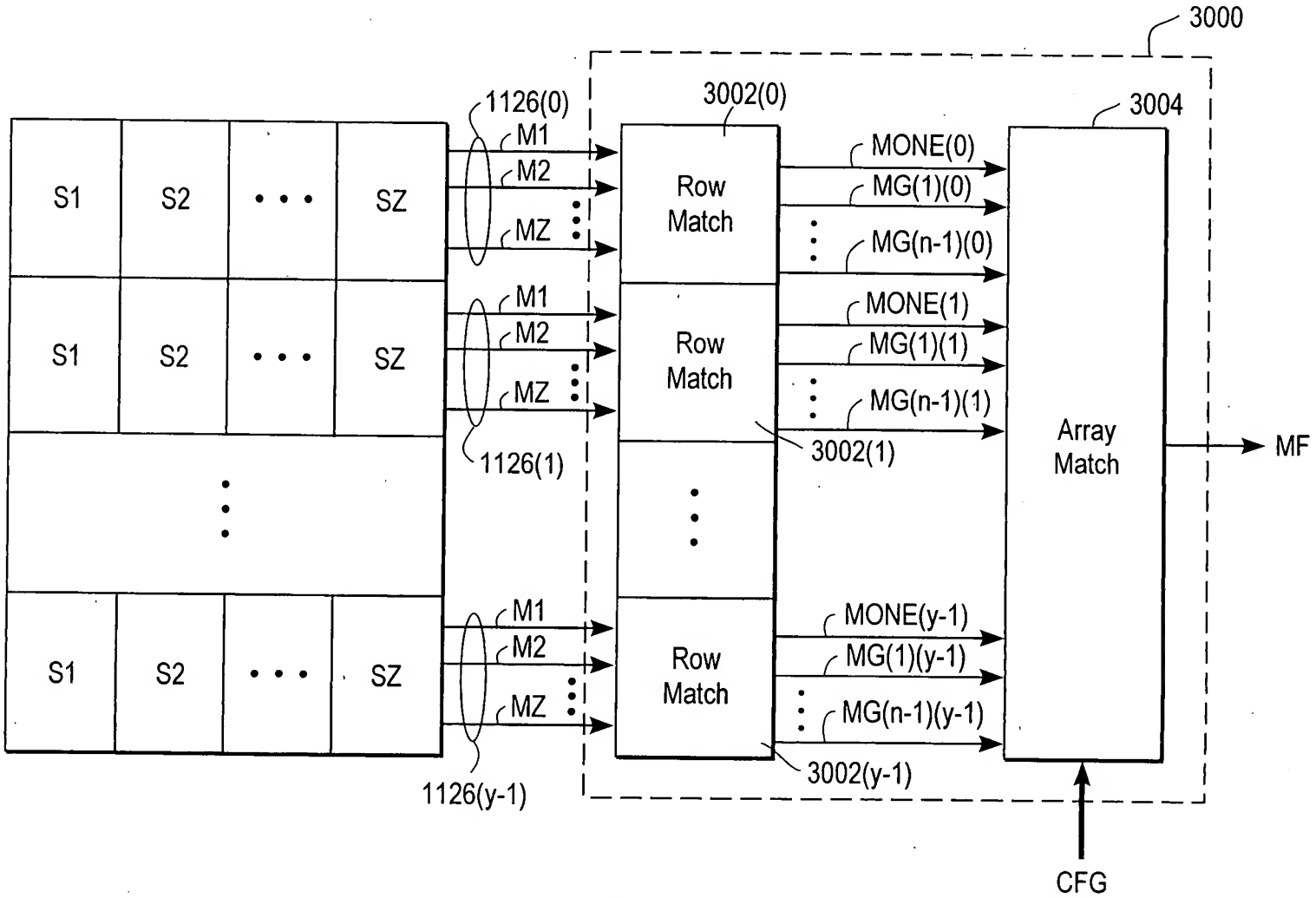

3000
1126(0)
3002(0)
3004
S1
S2
SZ
M1
M2
MZ
Row Match
MONE(0)
MG(1)(0)
MG(n-1)(0)
MONE(1)
MG(1)(1)
MG(n-1)(1)
1126(1)
3002(1)
Array Match
MF
MONE(y-1)
MG(1)(y-1)
MG(n-1)(y-1)
1126(y-1)
3002(y-1)
CFG

FIG. 32

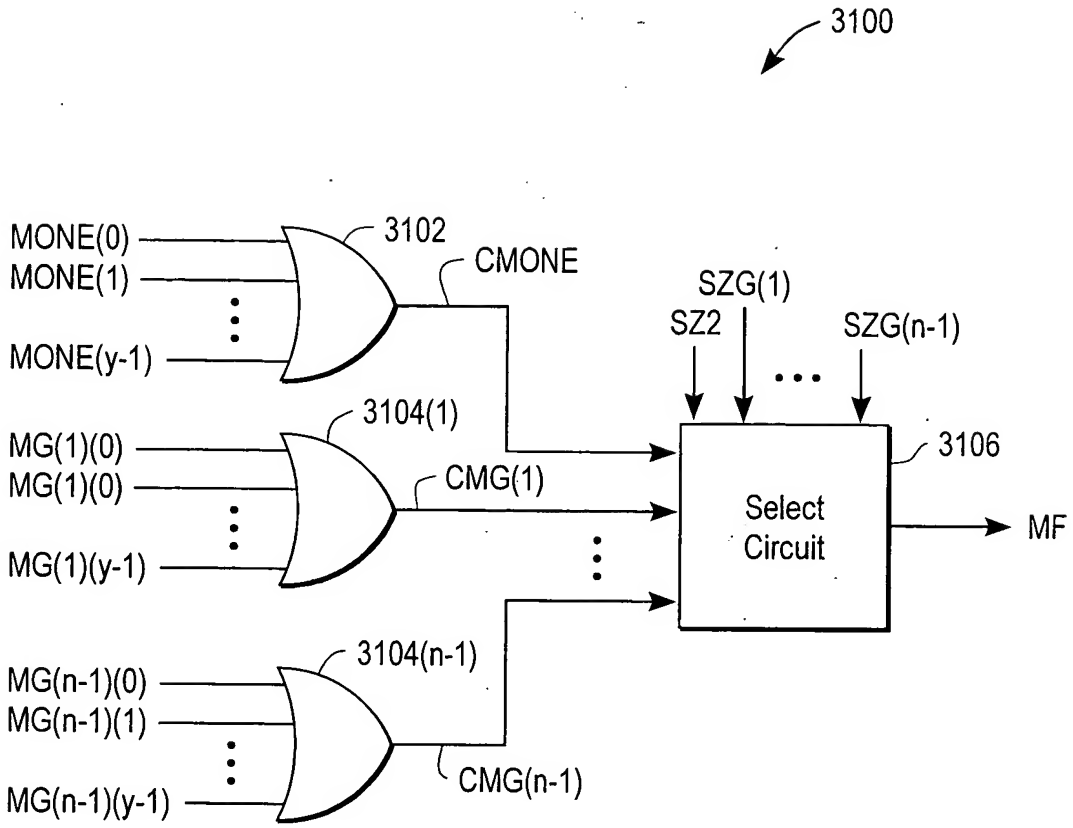

3100
MONE(0)
MONE(1)
MONE(y-1)
3102
CMONE
SZG(1)
SZ2
SZG(n-1)
MG(1)(0)
MG(1)(0)
MG(1)(y-1)
3104(1)
CMG(1)
3106
Select Circuit
MF
MG(n-1)(0)
MG(n-1)(1)
MG(n-1)(y-1)
3104(n-1)
CMG(n-1)

FIG. 33

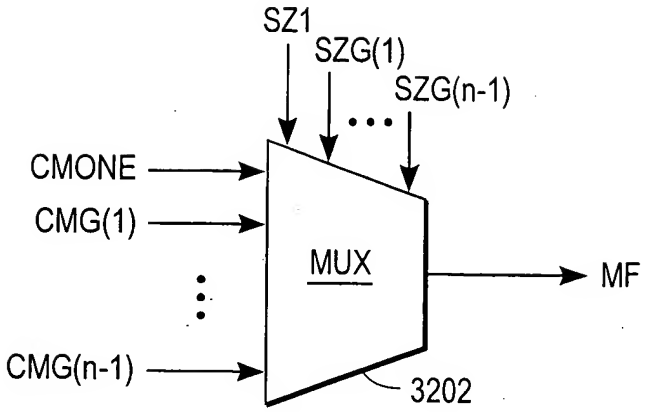

SZ1
SZG(1)
SZG(n-1)
CMONE
CMG(1)
MUX
MF
CMG(n-1)
3202

FIG. 34

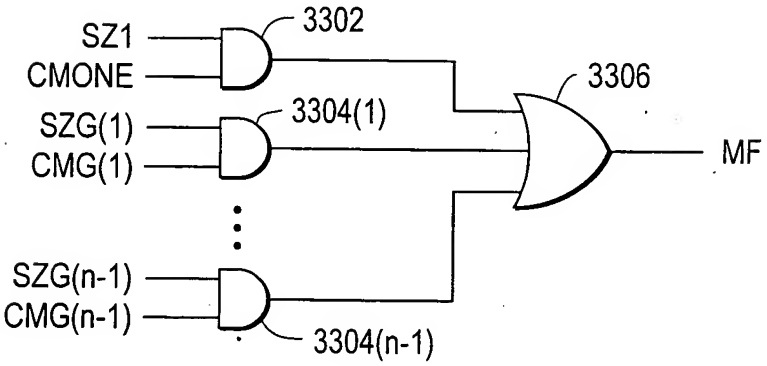

SZ1
CMONE
3302
SZG(1)
CMG(1)
3304(1)
3306
MF
SZG(n-1)
CMG(n-1)
3304(n-1)

FIG. 35

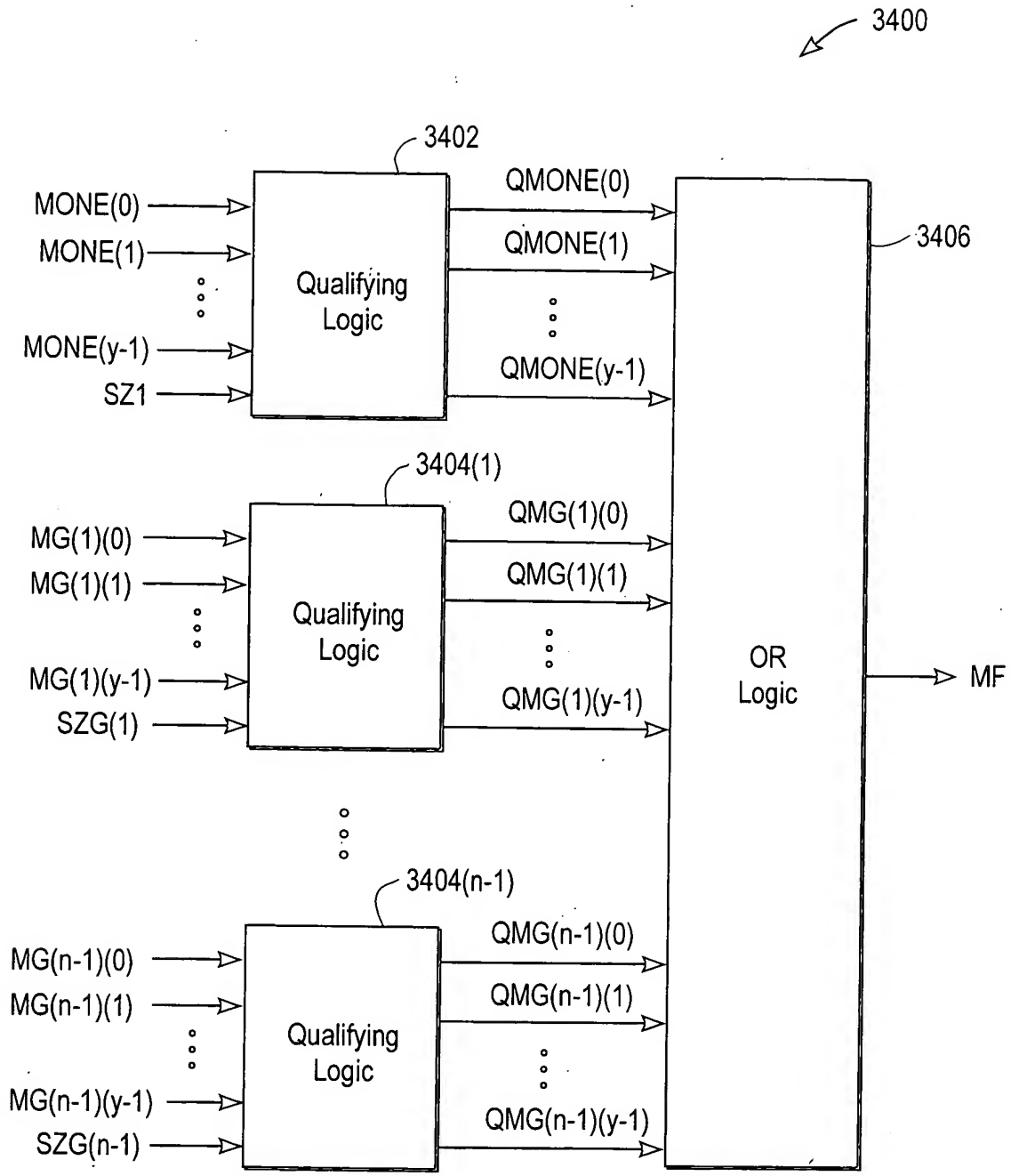

3400
3402
MONE(0)
MONE(1)
MONE(y-1)
SZ1
Qualifying Logic
QMONE(0)
QMONE(1)
QMONE(y-1)
3406
3404(1)
MG(1)(0)
MG(1)(1)
MG(1)(y-1)
SZG(1)
Qualifying Logic
QMG(1)(0)
QMG(1)(1)
QMG(1)(y-1)
OR Logic
MF
3404(n-1)
MG(n-1)(0)
MG(n-1)(1)
MG(n-1)(y-1)
SZG(n-1)
Qualifying Logic
QMG(n-1)(0)
QMG(n-1)(1)
QMG(n-1)(y-1)

FIG. 36

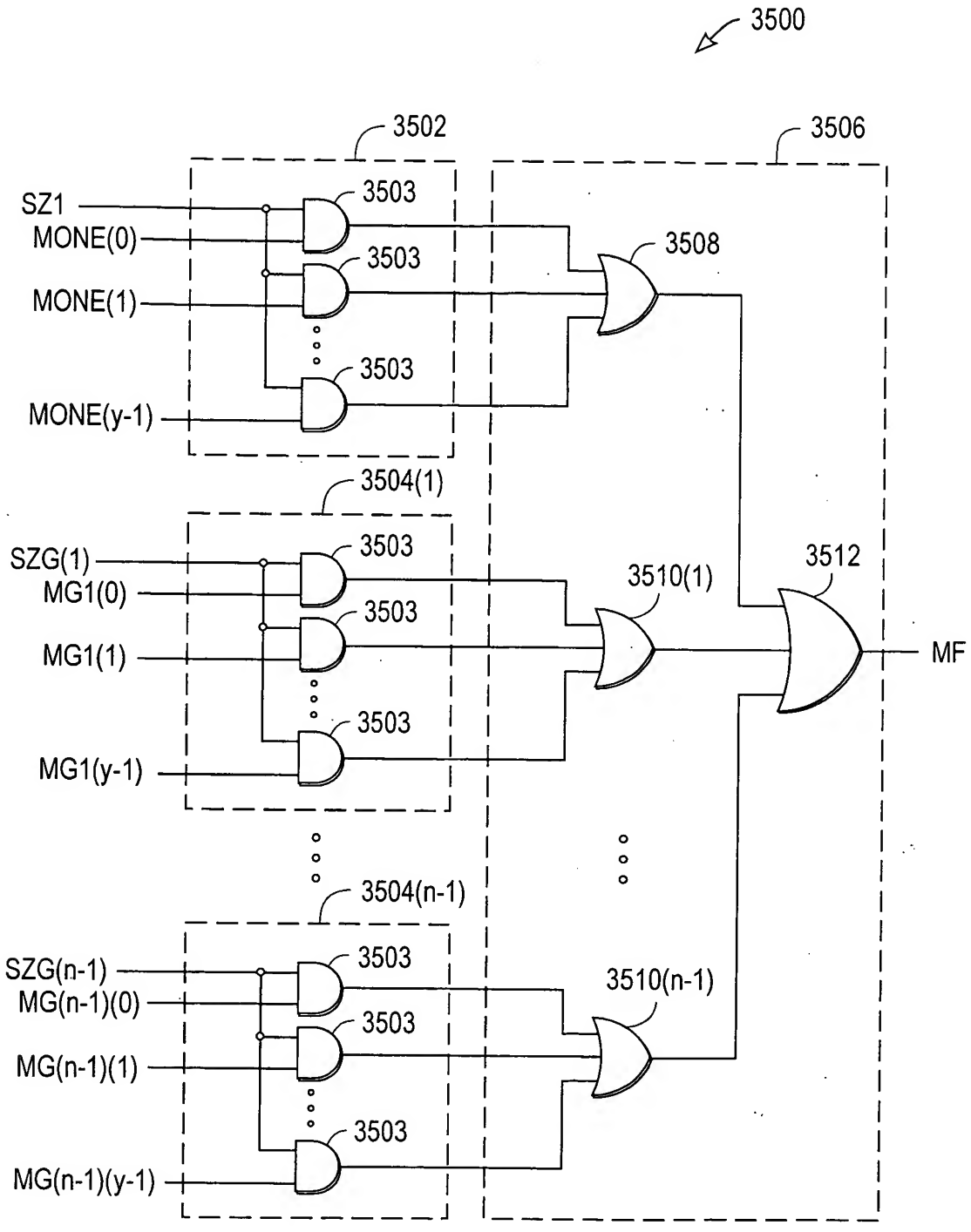

3500
3502
3506
SZ1
MONE(0)
MONE(1)
MONE(y-1)
3503
3503
3503
3508
3504(1)
SZG(1)
MG1(0)
MG1(1)
MG1(y-1)
3503
3503
3503
3510(1)
3512
MF
3504(n-1)
SZG(n-1)
MG(n-1)(0)
MG(n-1)(1)
MG(n-1)(y-1)
3503
3503
3503
3510(n-1)

FIG. 37

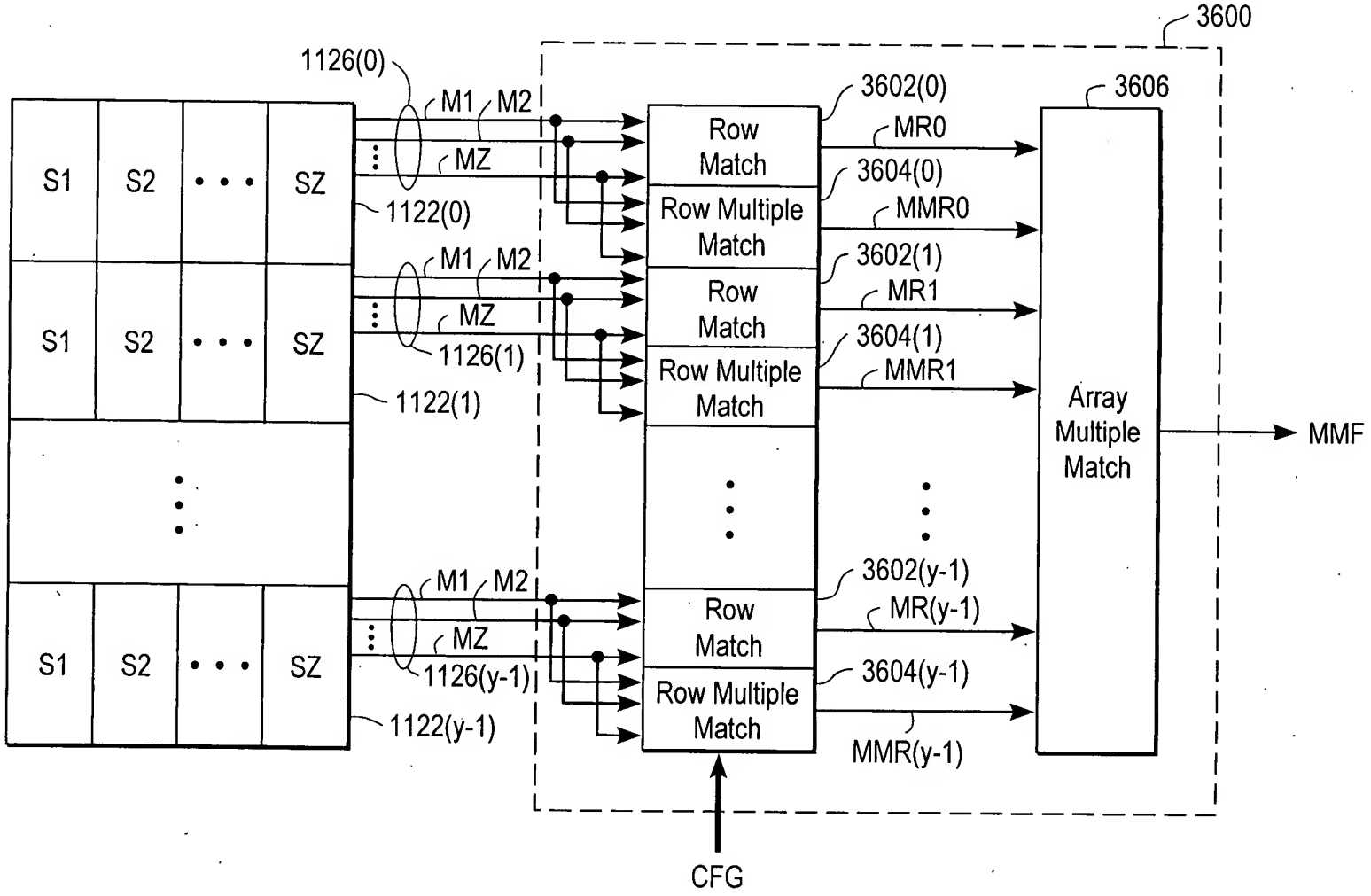

3600
1126(0)
M1
M2
MZ
1122(0)
S1
S2
SZ
1126(1)
1122(1)
1126(y-1)
1122(y-1)
Row Match
Row Multiple Match
3602(0)
MR0
3604(0)
MMR0
3602(1)
MR1
3604(1)
MMR1
3602(y-1)
MR(y-1)
3604(y-1)
MMR(y-1)
3606
Array Multiple Match
MMF
CFG

FIG. 38

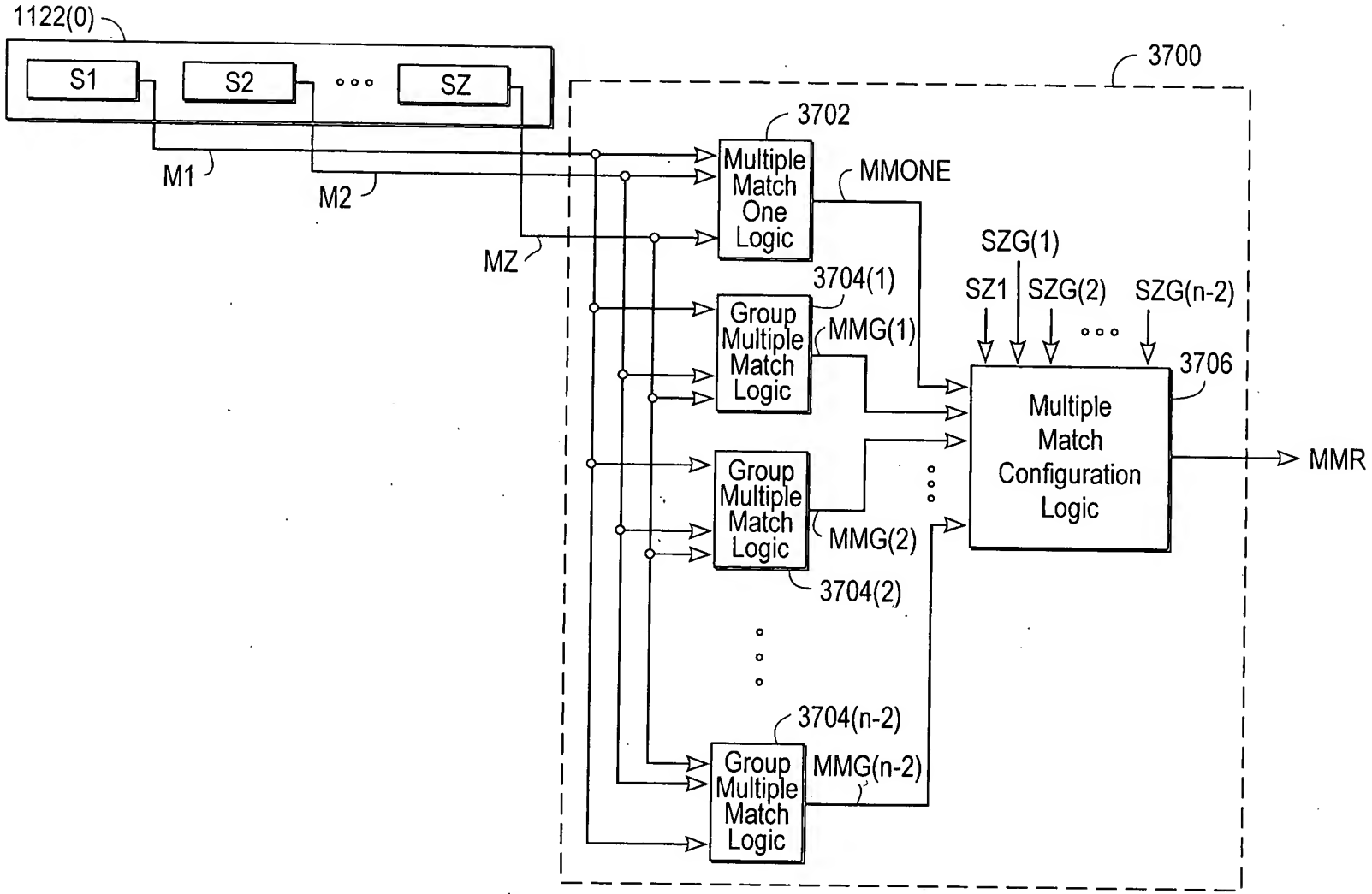

1122(0)
S1
S2
SZ
M1
M2
MZ
3700
3702
Multiple Match One Logic
MMONE
SZG(1)
SZ1
SZG(2)
SZG(n-2)
3704(1)
Group Multiple Match Logic
MMG(1)
3706
Multiple Match Configuration Logic
MMR
Group Multiple Match Logic
MMG(2)
3704(2)
3704(n-2)
Group Multiple Match Logic
MMG(n-2)

FIG. 39

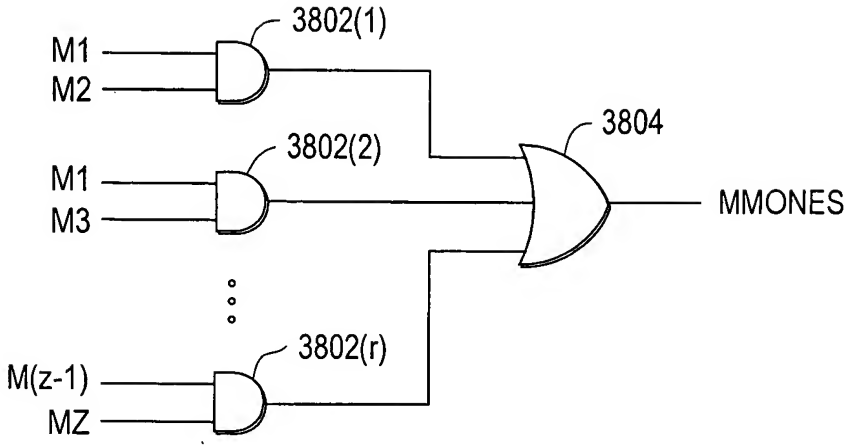

3802(1)
M1
M2
3804
3802(2)
M1
M3
MMONES
3802(r)
M(z-1)
MZ

FIG. 40

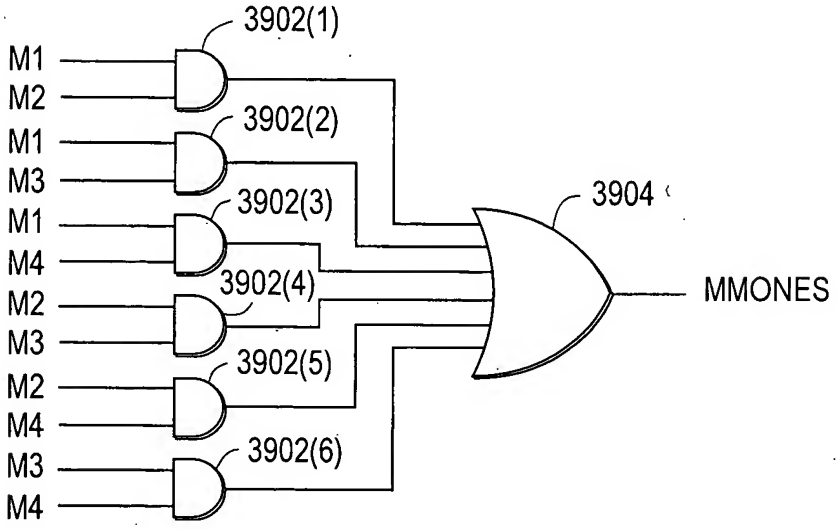

3902(1)
M1
M2
3902(2)
M1
M3
3902(3)
M1
M4
3904
3902(4)
M2
M3
MMONES
3902(5)
M2
M4
3902(6)
M3
M4

FIG. 41

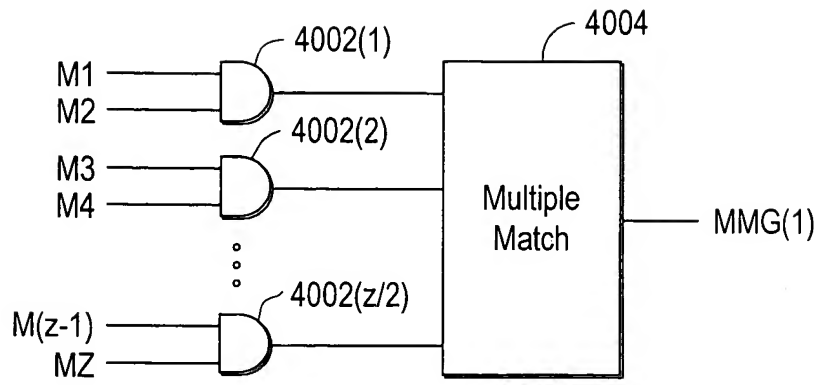


FIG. 42A

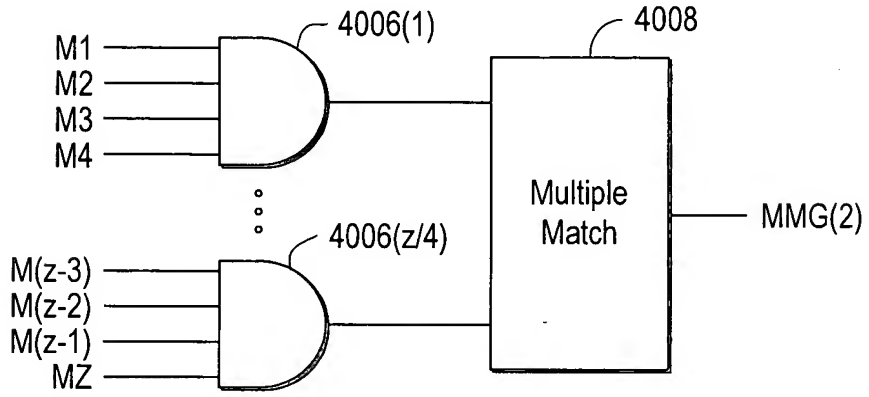


FIG. 42B

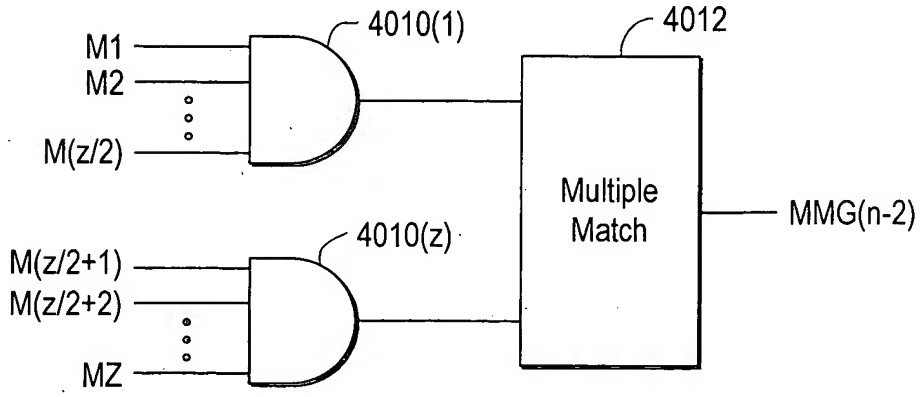


FIG. 42C

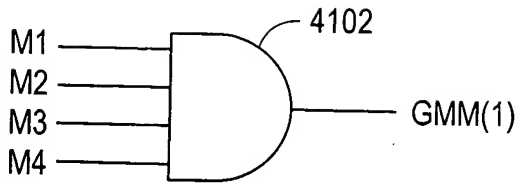


FIG. 43

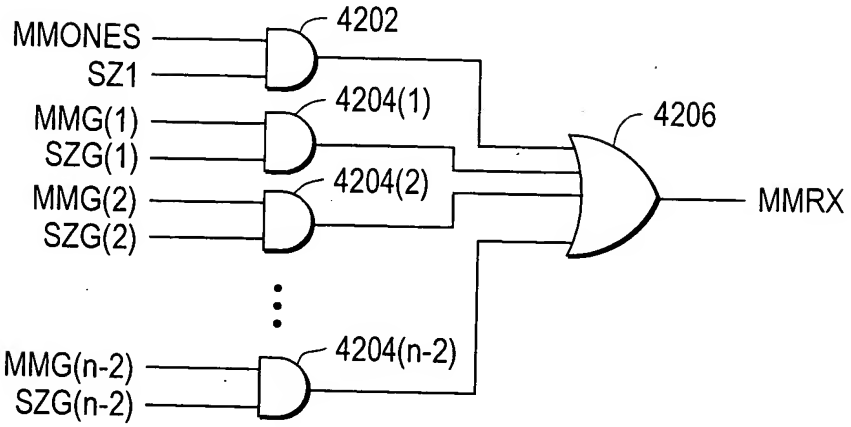


FIG. 44

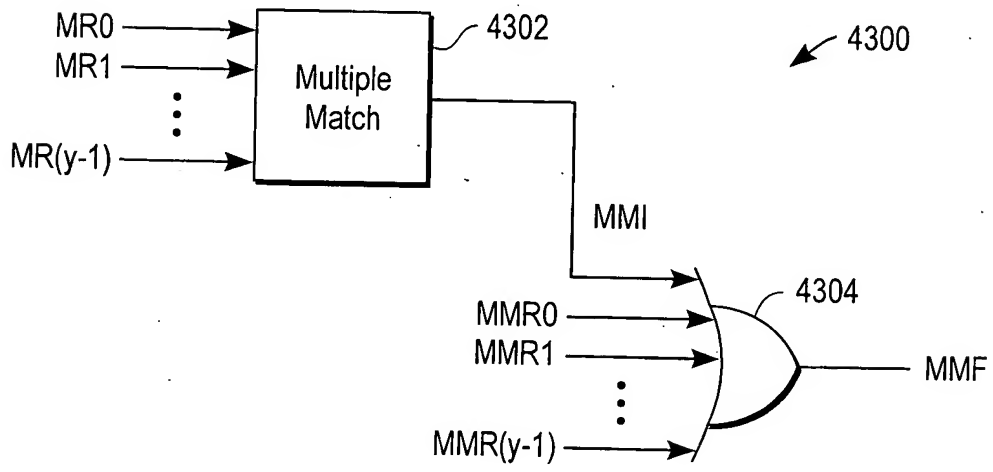


FIG. 45

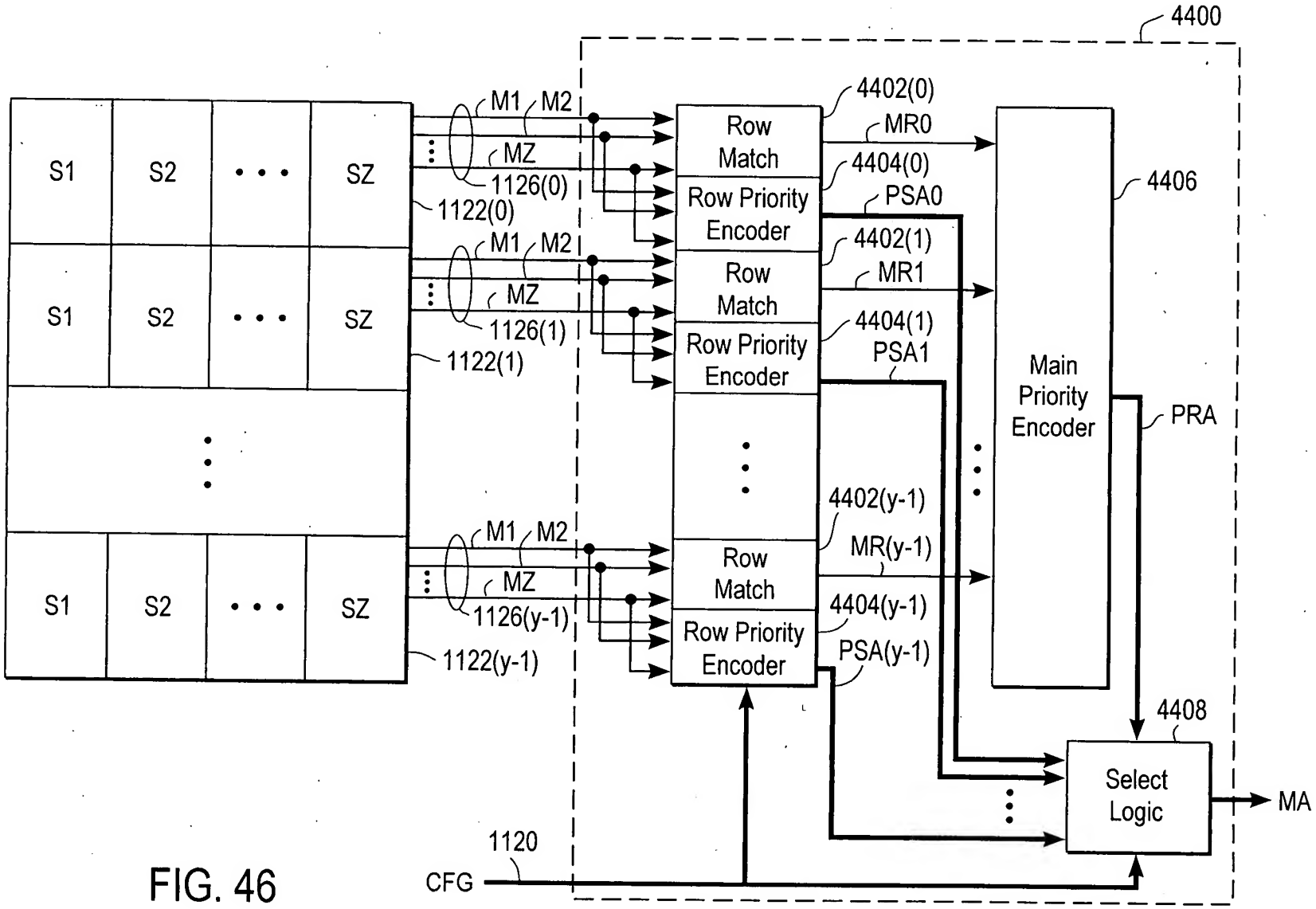

4400
S1
S2
SZ
M1
M2
MZ
1126(0)
1122(0)
1126(1)
1122(1)
1126(y-1)
1122(y-1)
Row Match
Row Priority Encoder
4402(0)
MR0
4404(0)
PSA0
4402(1)
MR1
4404(1)
PSA1
4402(y-1)
MR(y-1)
4404(y-1)
PSA(y-1)
Main Priority Encoder
4406
PRA
4408
Select Logic
MA
1120
CFG

FIG. 46

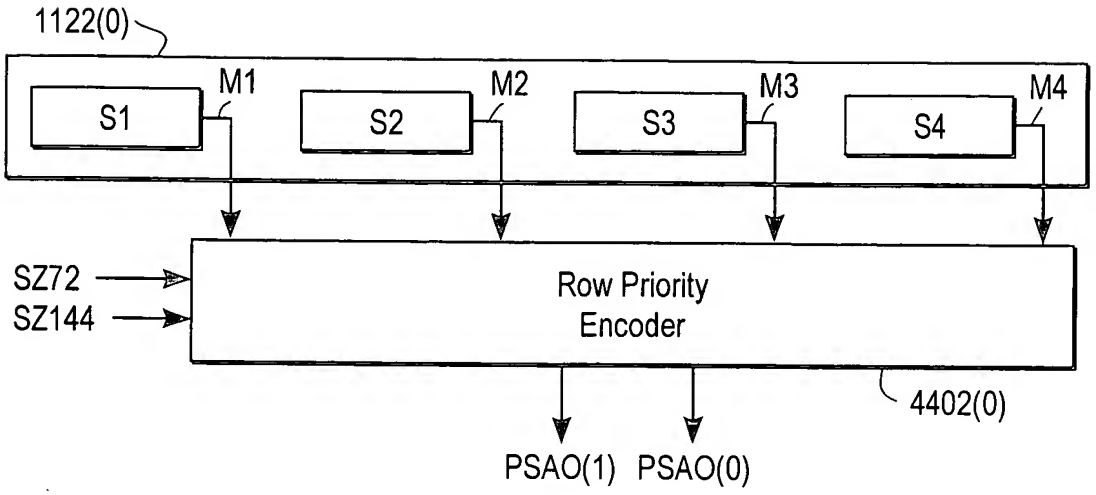


FIG. 47

M1	M2	M3	M4	ADDR	PSAO(1)	PSAO(0)
0	0	0	0	X	X	X
0	0	0	1	3	1	1
0	0	1	0	2	1	0
0	0	1	1	2	1	0
0	1	0	0	1	0	1
0	1	0	1	1	0	1
0	1	1	0	1	0	1
0	1	1	1	1	0	1
1	0	0	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	0	0	0
1	0	1	1	0	0	0
1	1	0	0	0	0	0
1	1	0	1	0	0	0
1	1	1	0	0	0	0
1	1	1	1	0	0	0

FIG. 48

M1	M2	M3	M4	ADDR	PSAO(1)	PSAO(0)
0	0	0	0	X	X	X
0	0	0	1	0	X	X
0	0	1	0	0	X	X
0	0	1	1	1	1	X
0	1	0	0	0	X	X
0	1	0	1	0	X	X
0	1	1	0	0	X	X
0	1	1	1	1	1	X
1	0	0	0	0	X	X
1	0	0	1	0	X	X
1	0	1	0	0	X	X
1	0	1	1	1	1	X
1	1	0	0	0	0	X
1	1	0	1	0	0	X
1	1	1	0	0	0	X
1	1	1	1	0	0	X

FIG. 49

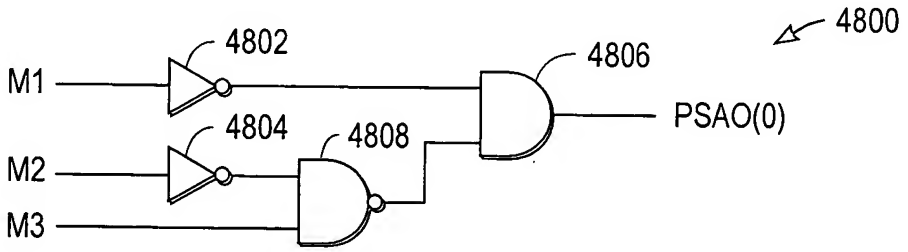


FIG. 50

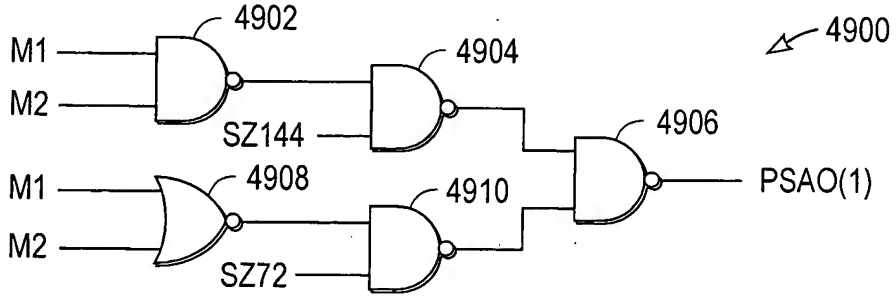


FIG. 51

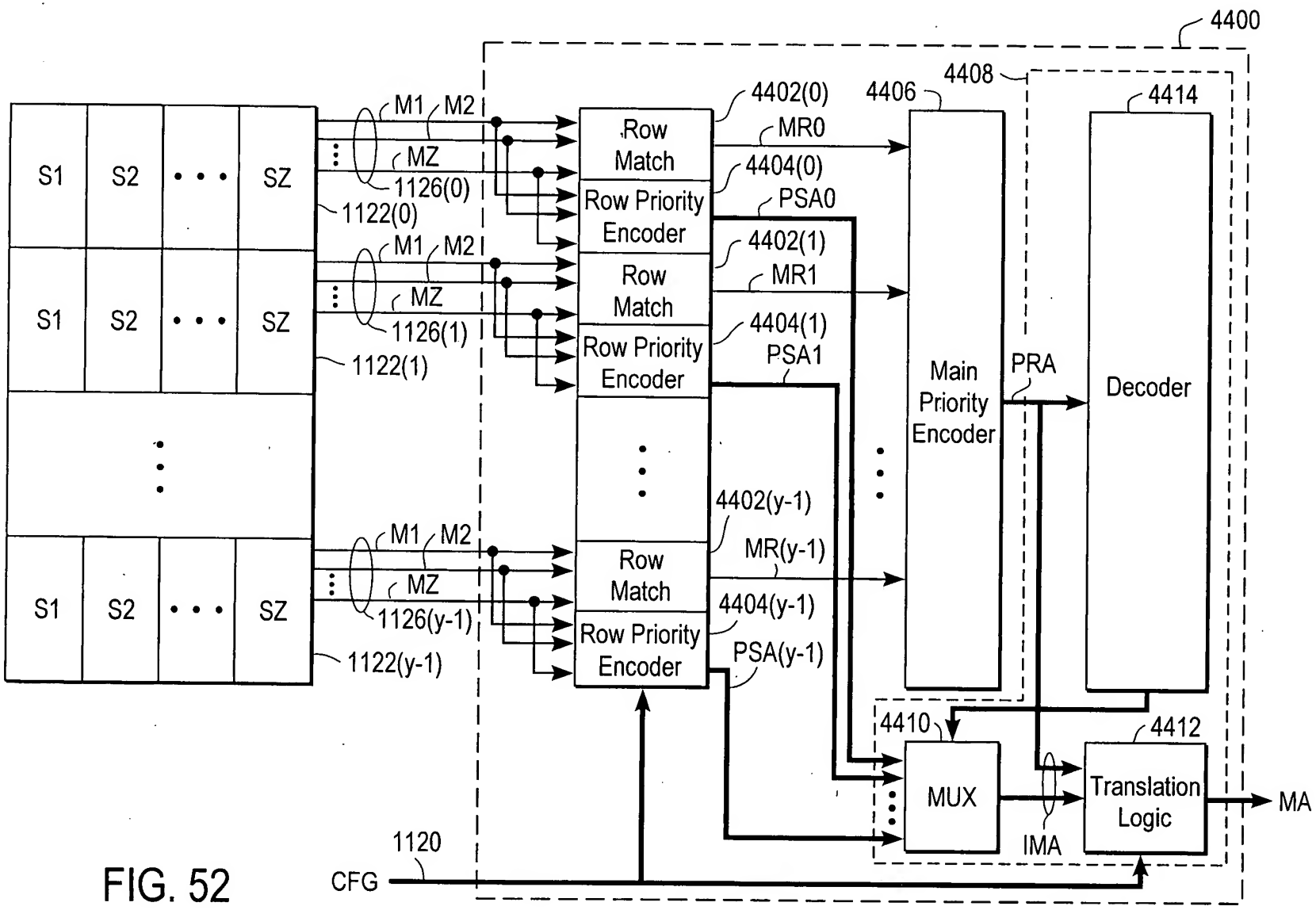

4400
4408
4406
4414
S1
S2
SZ
M1
M2
MZ
1126(0)
1122(0)
1126(1)
1122(1)
1126(y-1)
1122(y-1)
Row Match
Row Priority Encoder
4402(0)
MR0
4404(0)
PSA0
4402(1)
MR1
4404(1)
PSA1
4402(y-1)
MR(y-1)
4404(y-1)
PSA(y-1)
Main Priority Encoder
PRA
Decoder
4410
4412
MUX
Translation Logic
MA
IMA
1120
CFG

FIG. 52

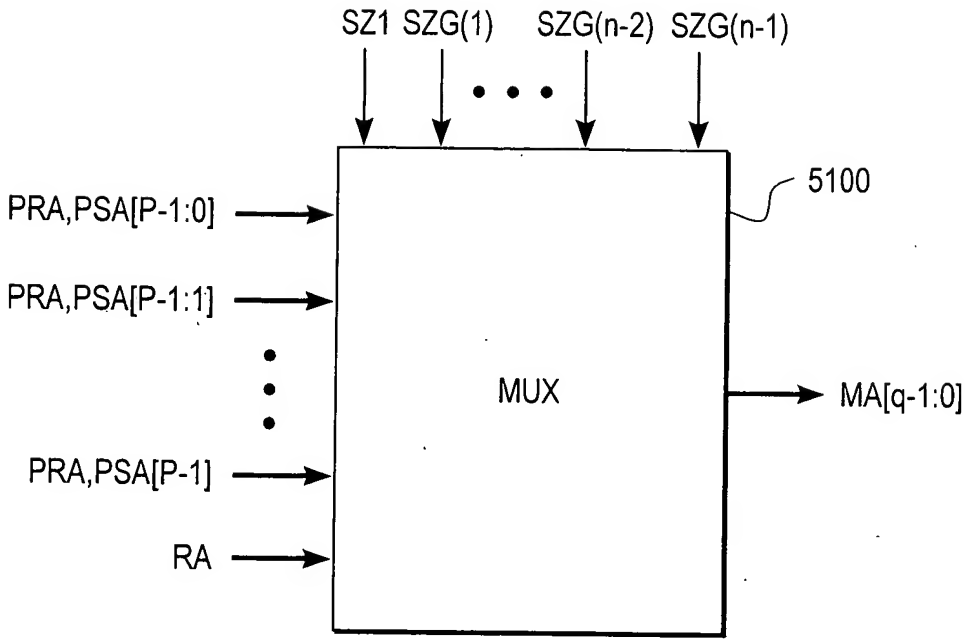

SZ1
SZG(1)
SZG(n-2)
SZG(n-1)
5100
PRA,PSA[P-1:0]
PRA,PSA[P-1:1]
PRA,PSA[P-1]
RA
MUX
MA[q-1:0]

FIG. 53

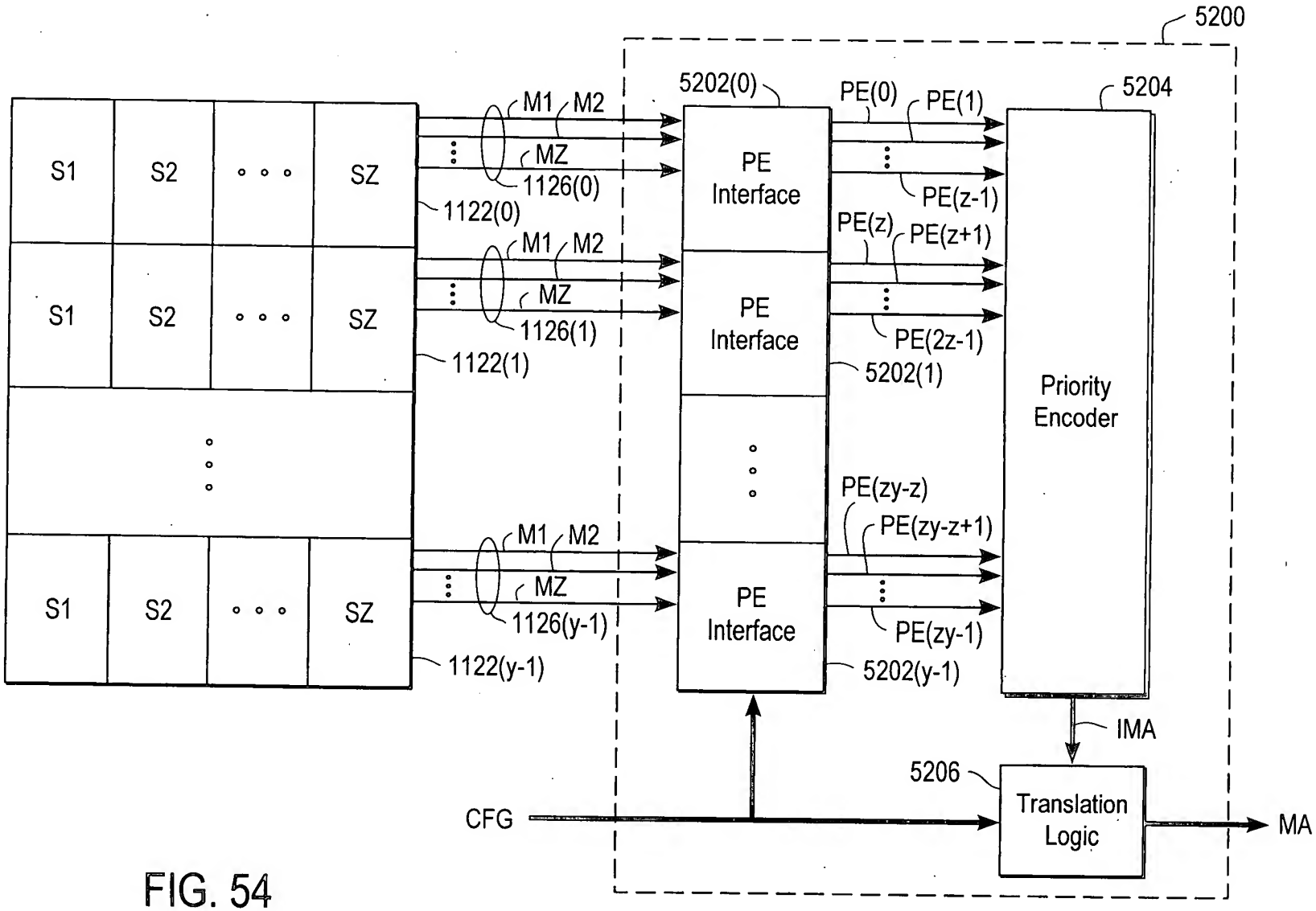

5200
S1
S2
SZ
1122(0)
1122(1)
1122(y-1)
M1
M2
MZ
1126(0)
1126(1)
1126(y-1)
5202(0)
PE Interface
5202(1)
5202(y-1)
PE(0)
PE(1)
PE(z-1)
PE(z)
PE(z+1)
PE(2z-1)
PE(zy-z)
PE(zy-z+1)
PE(zy-1)
5204
Priority Encoder
IMA
5206
Translation Logic
CFG
MA

FIG. 54

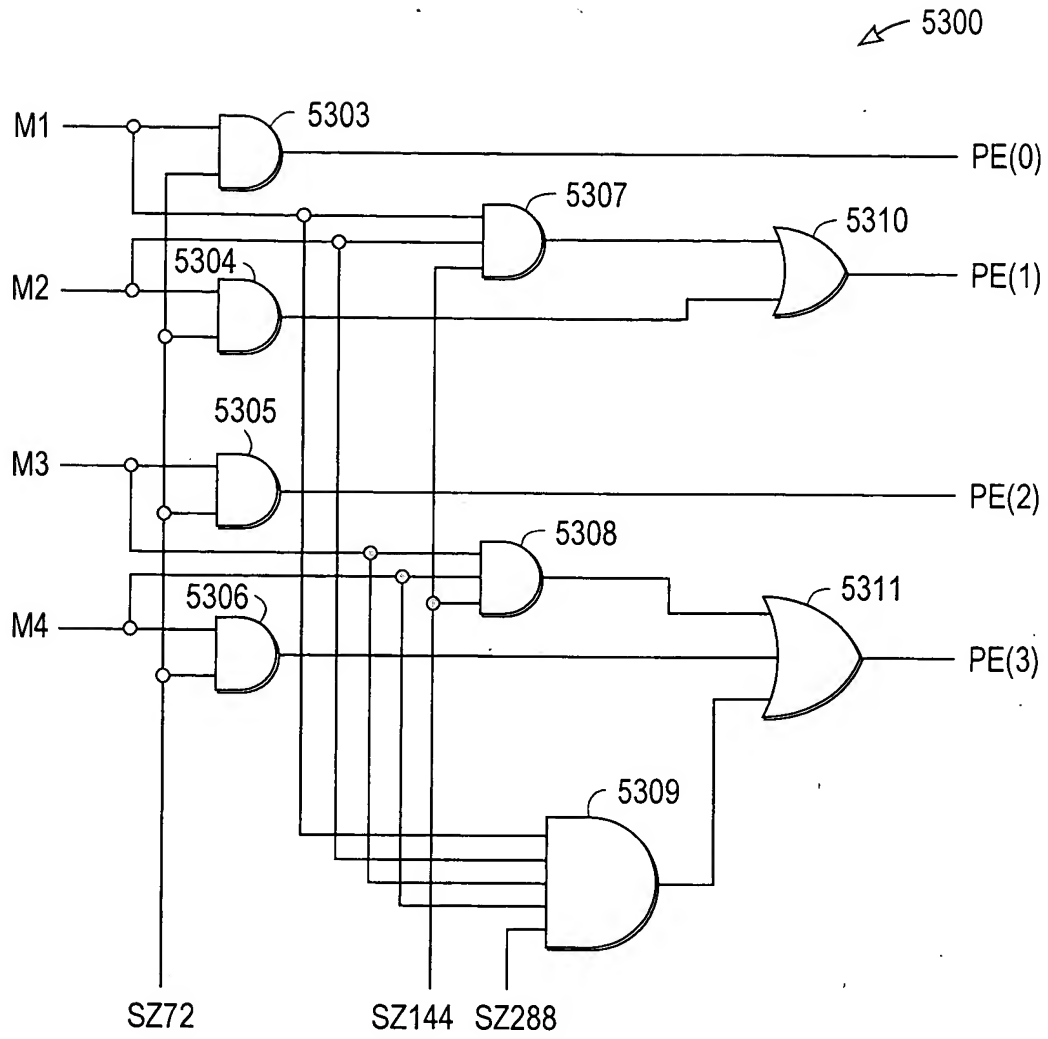

5300
M1
5303
PE(0)
5307
5310
M2
5304
PE(1)
5305
M3
PE(2)
5308
5311
M4
5306
PE(3)
5309
SZ72
SZ144
SZ288

FIG. 55

Configuration	PE Inputs
$ZY \times W$	Set to M1-MZ for Corresponding Rows
$\frac{ZY}{2} \times 2W$	Set Every 2nd PE Input to the Corresponding First Group Match Results; Set All Other PE Inputs to Mismatch
$\frac{ZY}{4} \times 4W$	Set Every 4th PE Input to the Corresponding Second Group Match Results; Set All Other PE Inputs to Mismatch
⋮	⋮
$\frac{ZY}{(z-1)} \times (z-1)W$	Set Every (z-1) PE Input to the Corresponding (z-1) Group Match Results; Set All Other PE Inputs to Mismatch
$Y \times ZW$	Set Every Zth PE Input to the Corresponding Row Group Match Results; Set All Other PE Inputs to Mismatch

FIG. 56

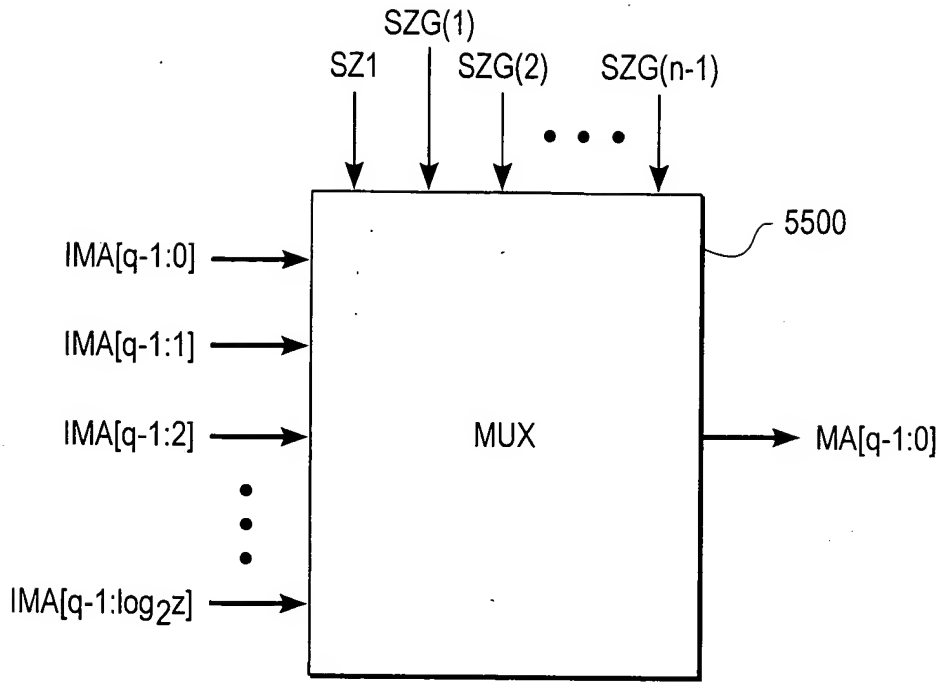

SZG(1)
SZ1
SZG(2)
SZG(n-1)
5500
IMA[q-1:0]
IMA[q-1:1]
IMA[q-1:2]
IMA[q-1:log2z]
MUX
MA[q-1:0]

FIG. 57

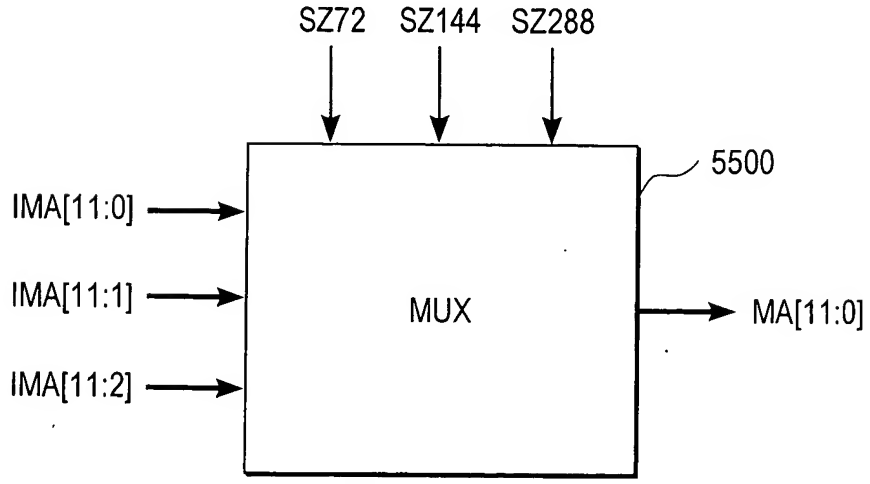

SZ72
SZ144
SZ288
5500
IMA[11:0]
IMA[11:1]
IMA[11:2]
MUX
MA[11:0]

FIG. 58

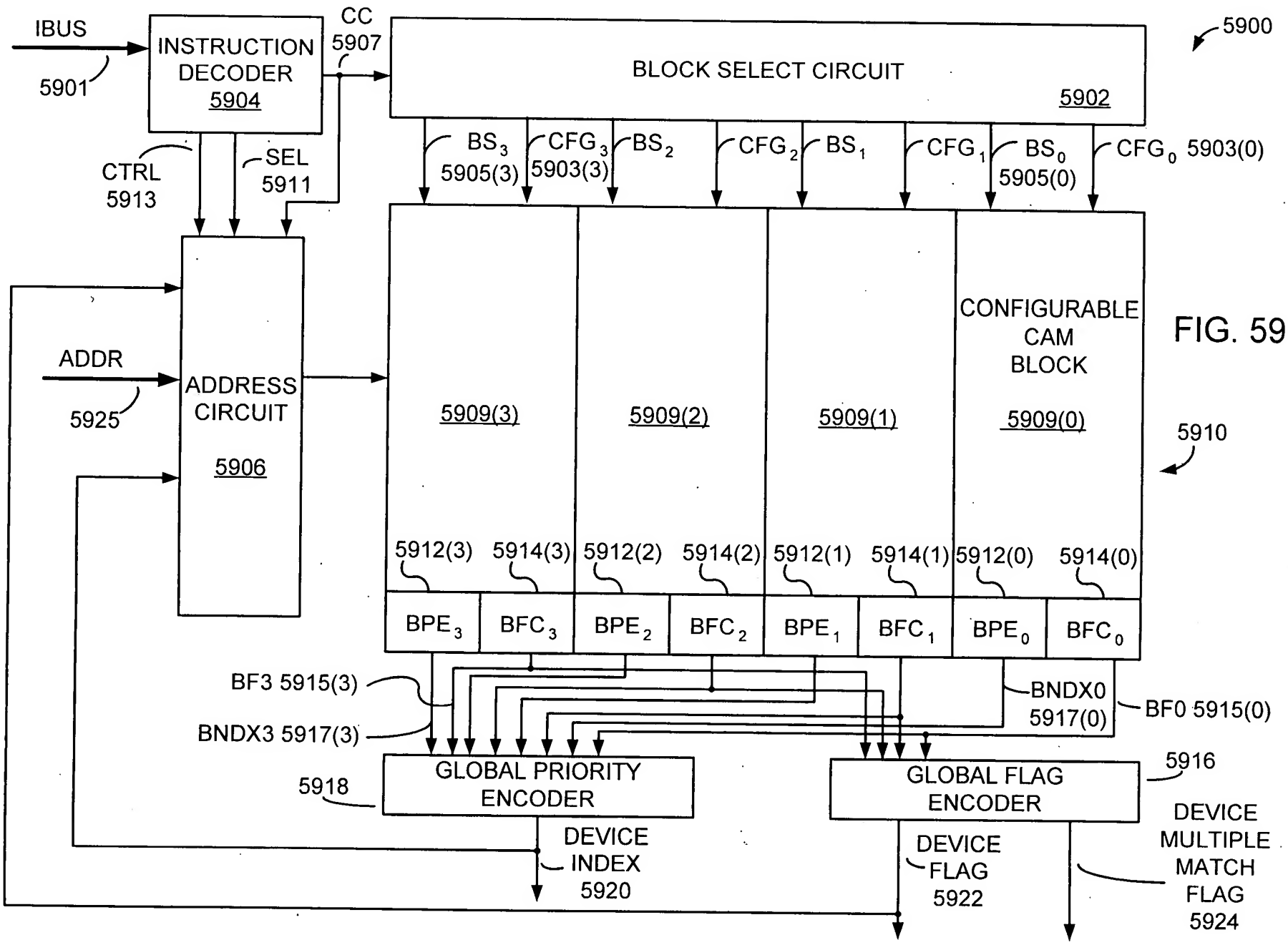

IBUS
5901
INSTRUCTION DECODER 5904
CC 5907
BLOCK SELECT CIRCUIT 5902
5900
CTRL 5913
SEL 5911
BS3 5905(3)
CFG3 5903(3)
BS2
CFG2
BS1
CFG1
BS0 5905(0)
CFG0 5903(0)
ADDR
5925
ADDRESS CIRCUIT 5906
5909(3)
5909(2)
5909(1)
CONFIGURABLE CAM BLOCK
5909(0)
5910
5912(3) 5914(3) 5912(2) 5914(2) 5912(1) 5914(1) 5912(0) 5914(0)
BPE3 BFC3 BPE2 BFC2 BPE1 BFC1 BPE0 BFC0
BF3 5915(3)
BNDX3 5917(3)
BNDX0 5917(0)
BF0 5915(0)
GLOBAL PRIORITY ENCODER
5918
GLOBAL FLAG ENCODER
5916
DEVICE INDEX 5920
DEVICE FLAG 5922
DEVICE MULTIPLE MATCH FLAG 5924

FIG. 59

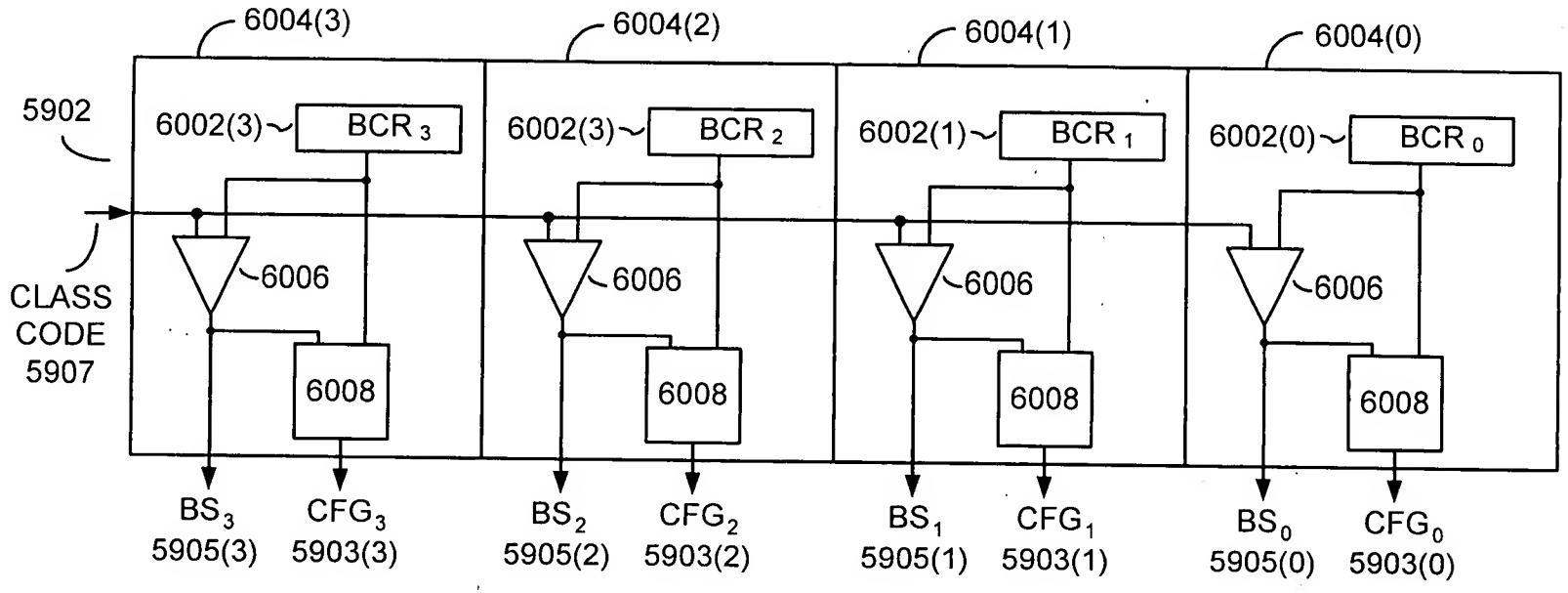

6004(3)
6004(2)
6004(1)
6004(0)
5902
6002(3)
BCR 3
6002(3)
BCR 2
6002(1)
BCR 1
6002(0)
BCR 0
CLASS CODE 5907
6006
6008
BS3 5905(3)
CFG3 5903(3)
BS2 5905(2)
CFG2 5903(2)
BS1 5905(1)
CFG1 5903(1)
BS0 5905(0)
CFG0 5903(0)

FIG. 60

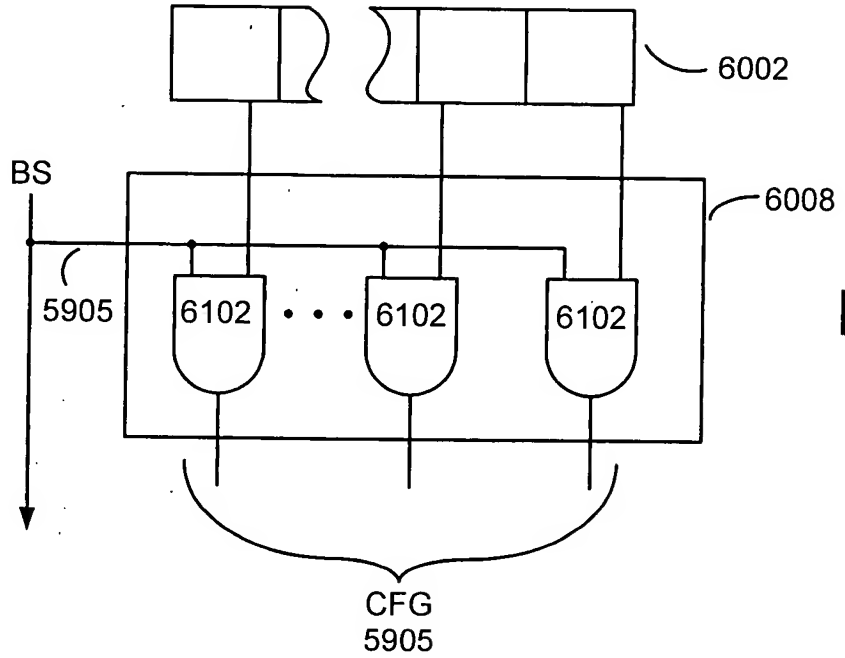

6002
BS
6008
5905
6102
6102
6102
CFG 5905

FIG. 61

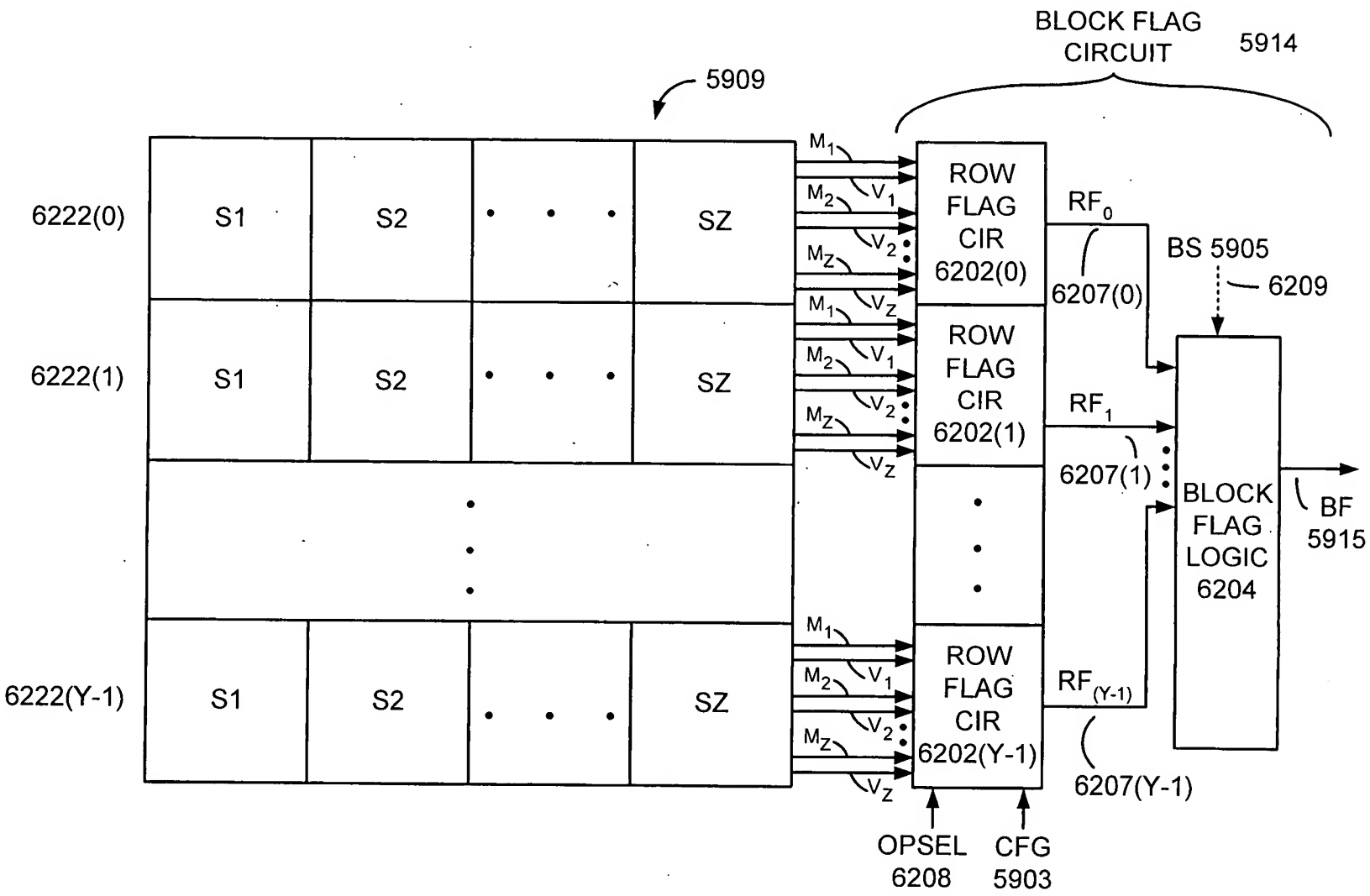

BLOCK FLAG CIRCUIT
5914
5909
6222(0)
6222(1)
6222(Y-1)
S1
S2
SZ
M1
M2
MZ
V1
V2
VZ
ROW FLAG CIR 6202(0)
ROW FLAG CIR 6202(1)
ROW FLAG CIR 6202(Y-1)
RF0
RF1
RF(Y-1)
6207(0)
6207(1)
6207(Y-1)
BS 5905
6209
BLOCK FLAG LOGIC 6204
BF 5915
OPSEL 6208
CFG 5903

FIG. 62

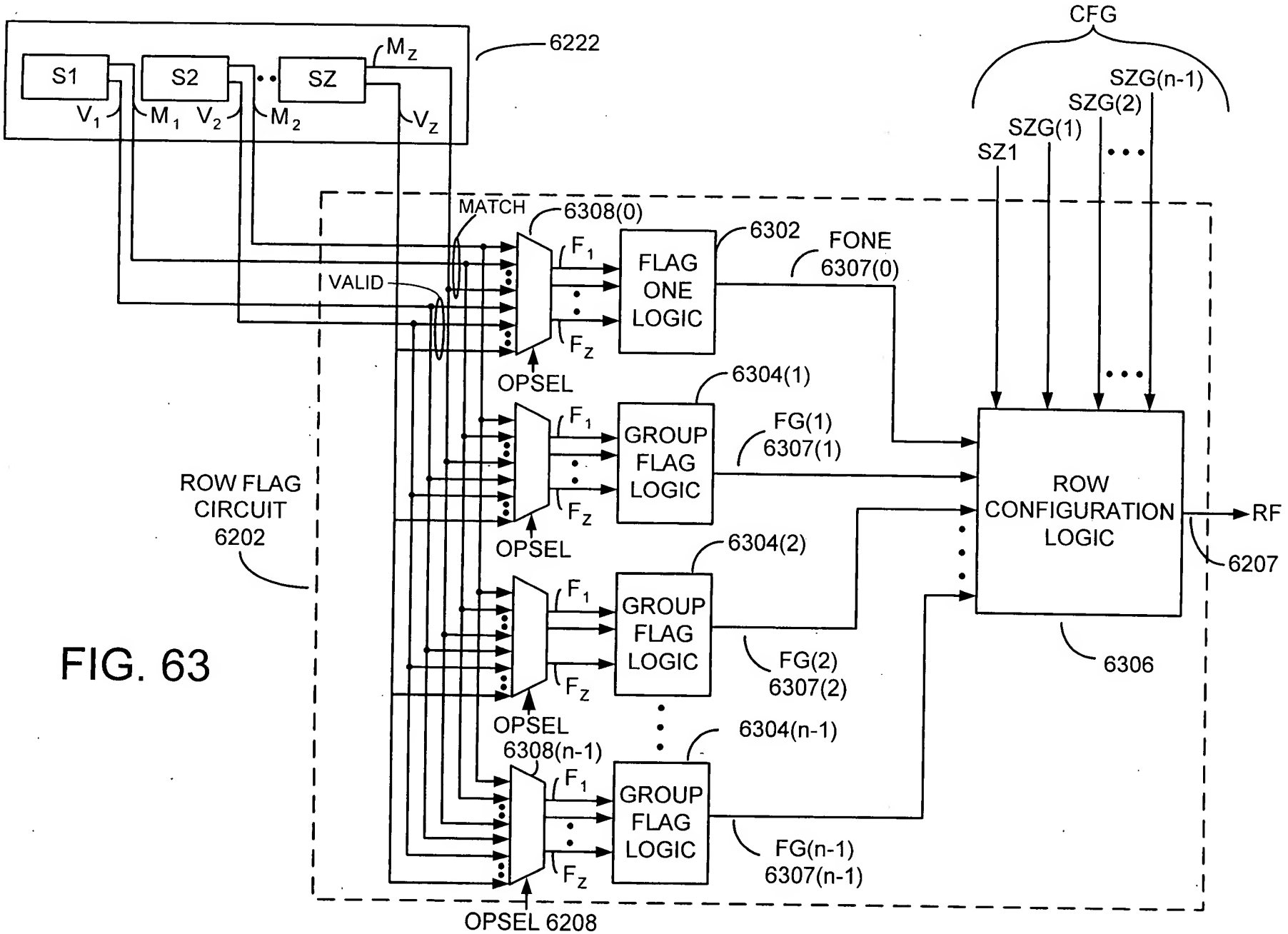
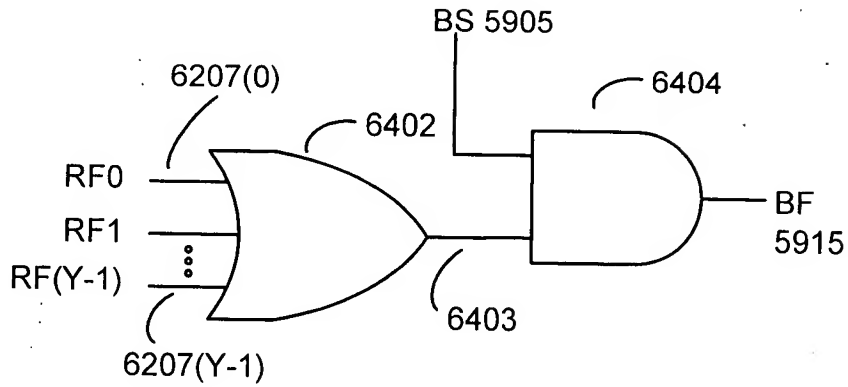

6222
S1
S2
SZ
M_Z
V_1
M_1
V_2
M_2
V_Z
CFG
SZG(n-1)
SZG(2)
SZG(1)
SZ1
MATCH
6308(0)
VALID
F_1
F_Z
OPSEL
6302
FONE
6307(0)
FLAG ONE LOGIC
6304(1)
GROUP FLAG LOGIC
FG(1)
6307(1)
6304(2)
FG(2)
6307(2)
6304(n-1)
6308(n-1)
FG(n-1)
6307(n-1)
OPSEL 6208
ROW FLAG CIRCUIT 6202
ROW CONFIGURATION LOGIC
RF
6207
6306

FIG. 63

FIG. 64


BS 5905
6207(0)
6404
6402
RF0
RF1
RF(Y-1)
BF
5915
6403
6207(Y-1)

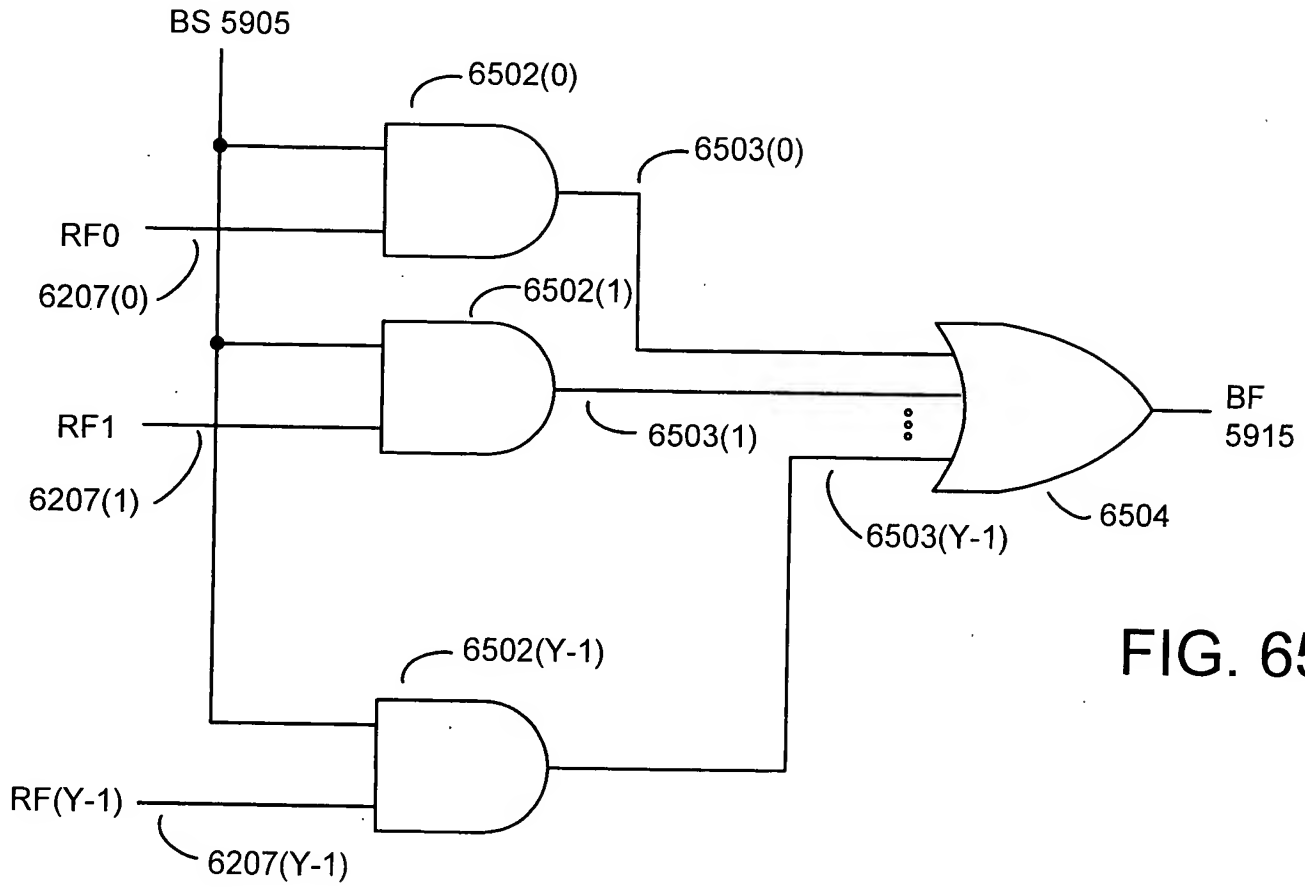

BS 5905
6502(0)
6503(0)
RF0
6207(0)
6502(1)
RF1
6503(1)
BF
5915
6207(1)
6504
6503(Y-1)
6502(Y-1)
RF(Y-1)
6207(Y-1)

FIG. 65

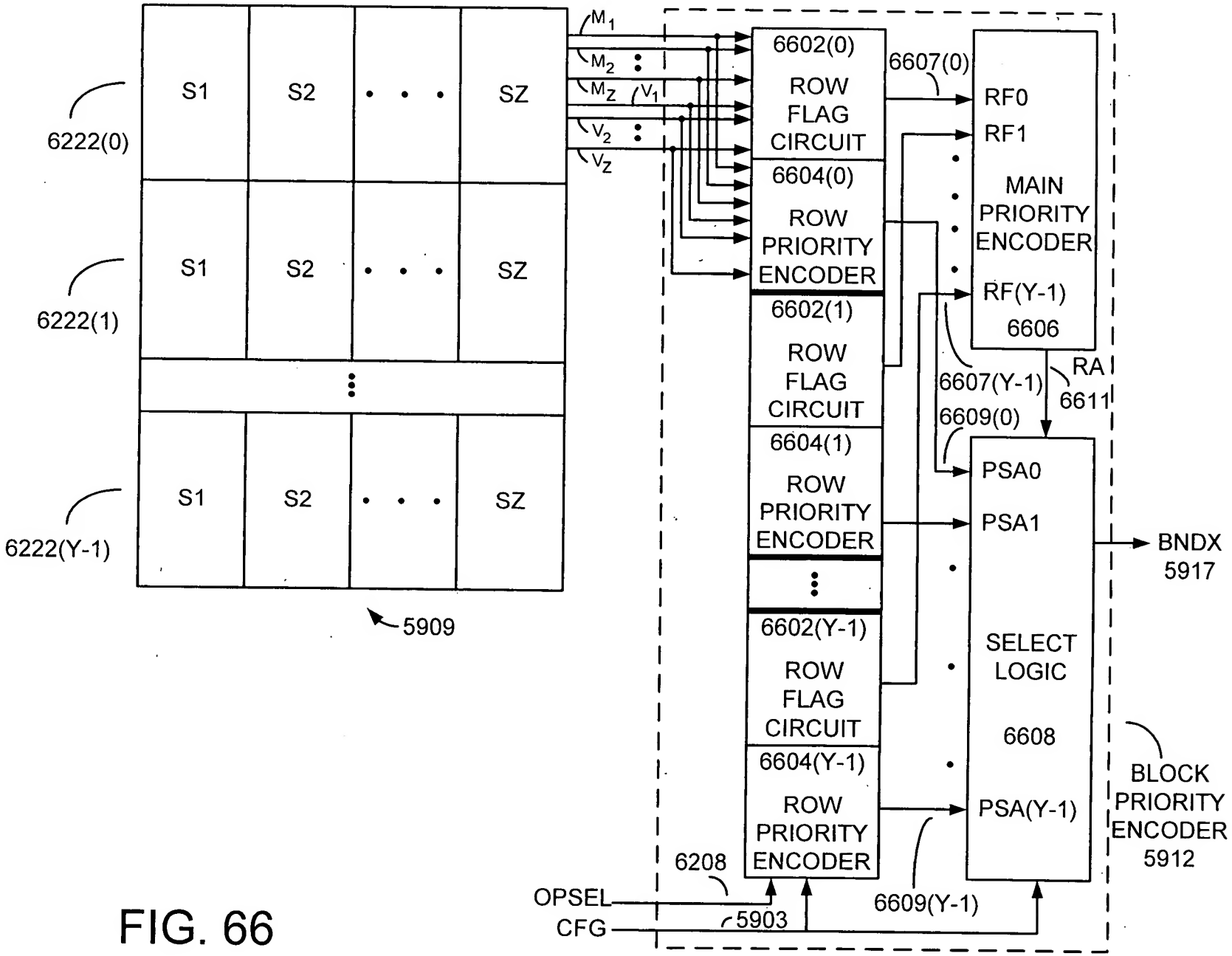

S1
S2
SZ
6222(0)
6222(1)
6222(Y-1)
5909
M1
M2
MZ
V1
V2
VZ
6602(0)
ROW FLAG CIRCUIT
6604(0)
ROW PRIORITY ENCODER
6602(1)
ROW FLAG CIRCUIT
6604(1)
ROW PRIORITY ENCODER
6602(Y-1)
ROW FLAG CIRCUIT
6604(Y-1)
ROW PRIORITY ENCODER
6607(0)
RF0
RF1
MAIN PRIORITY ENCODER
RF(Y-1)
6606
6607(Y-1)
RA
6611
6609(0)
PSA0
PSA1
SELECT LOGIC
6608
PSA(Y-1)
BNDX
5917
BLOCK PRIORITY ENCODER
5912
6609(Y-1)
6208
OPSEL
CFG
5903

FIG. 66

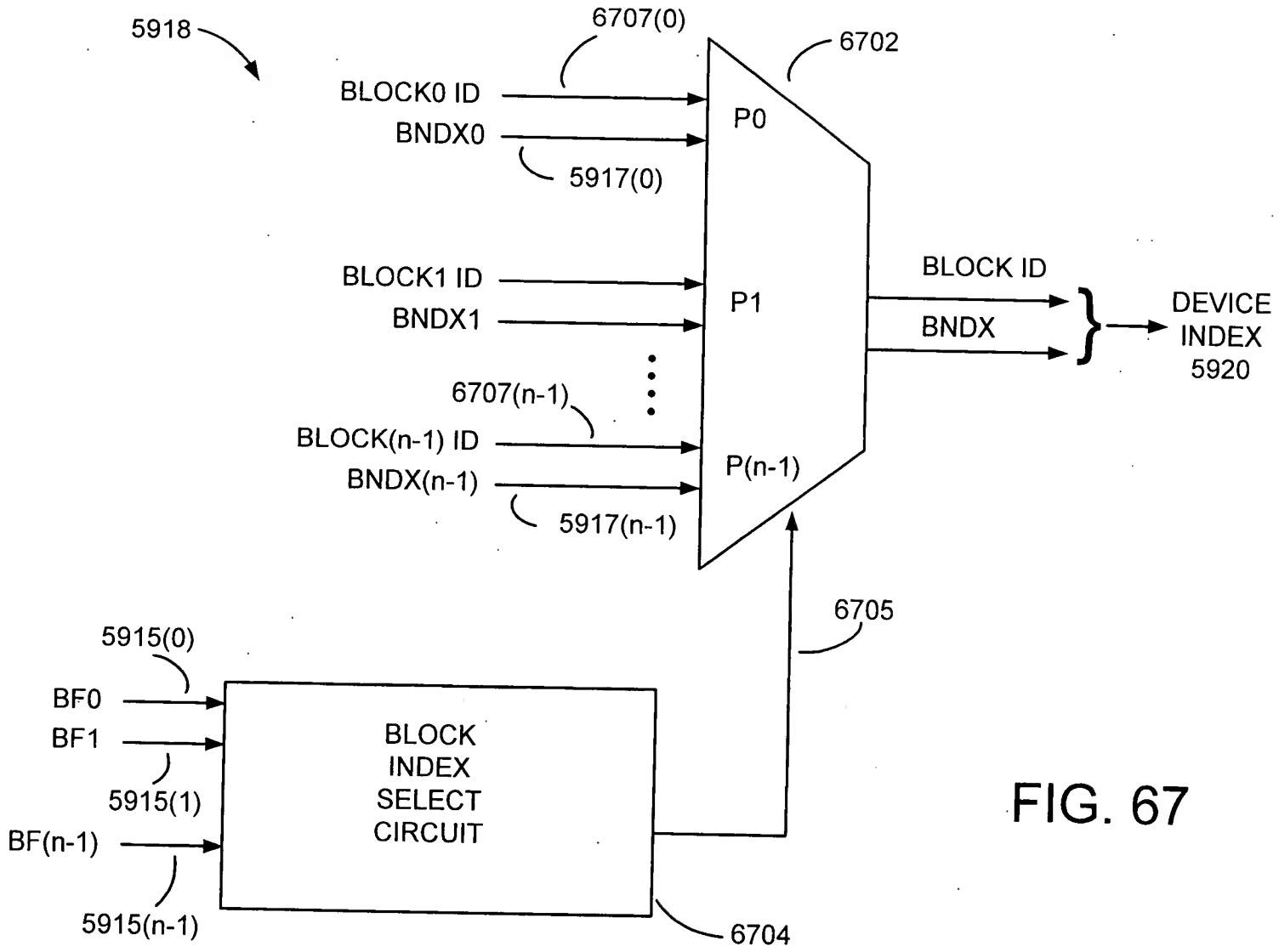

5918
6707(0)
6702
BLOCK0 ID
BNDX0
5917(0)
P0
BLOCK1 ID
BNDX1
P1
6707(n-1)
BLOCK(n-1) ID
BNDX(n-1)
5917(n-1)
P(n-1)
BLOCK ID
BNDX
DEVICE INDEX 5920
6705
5915(0)
BF0
BF1
5915(1)
BF(n-1)
5915(n-1)
BLOCK INDEX SELECT CIRCUIT
6704

FIG. 67

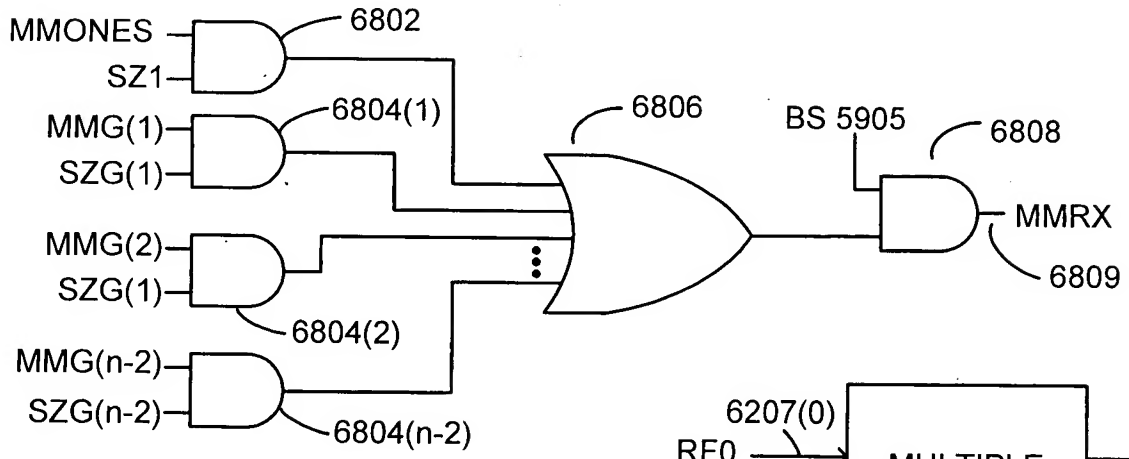


FIG. 68

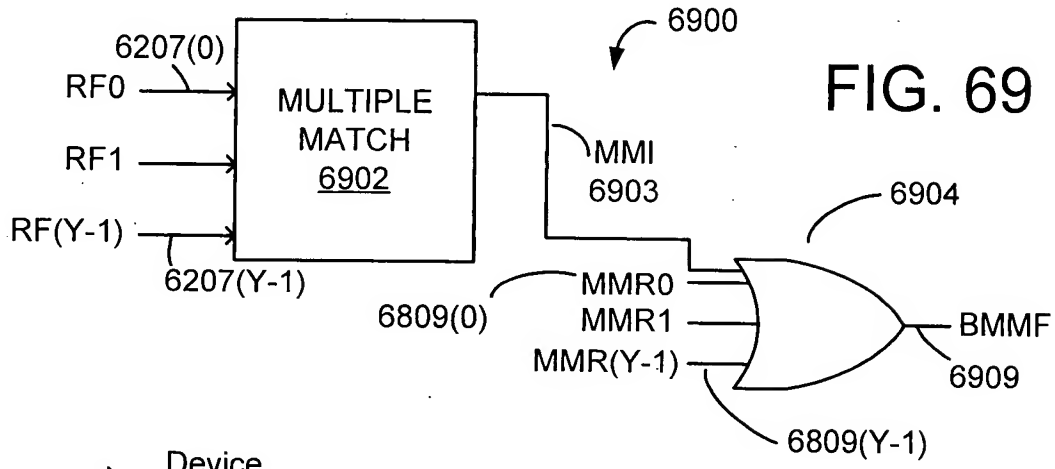


FIG. 69

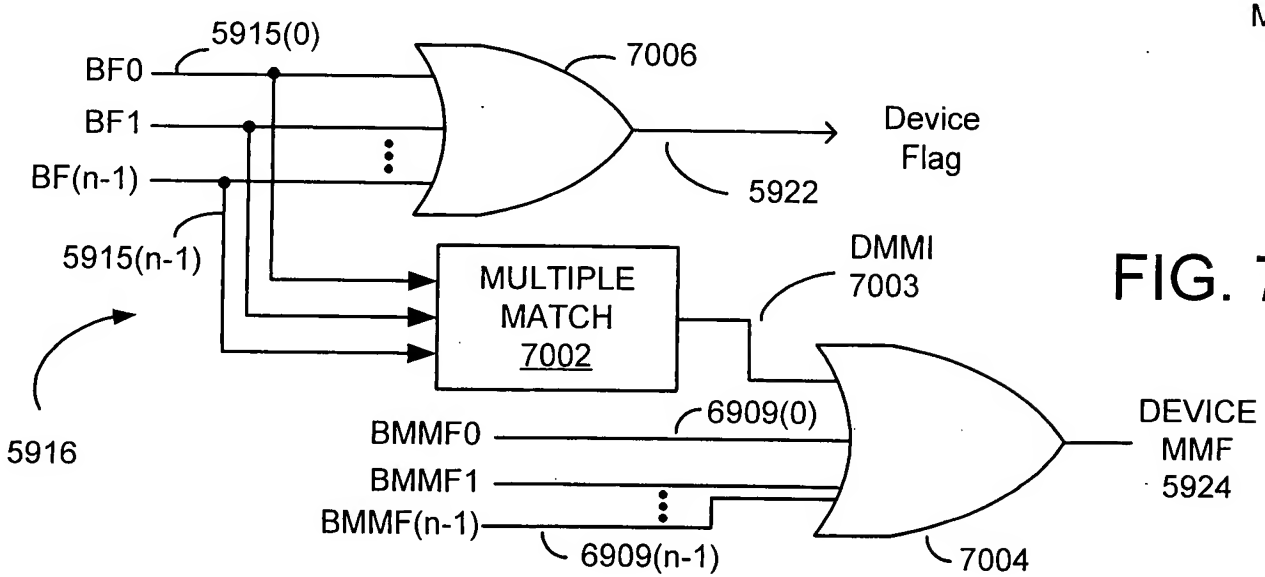


FIG. 70

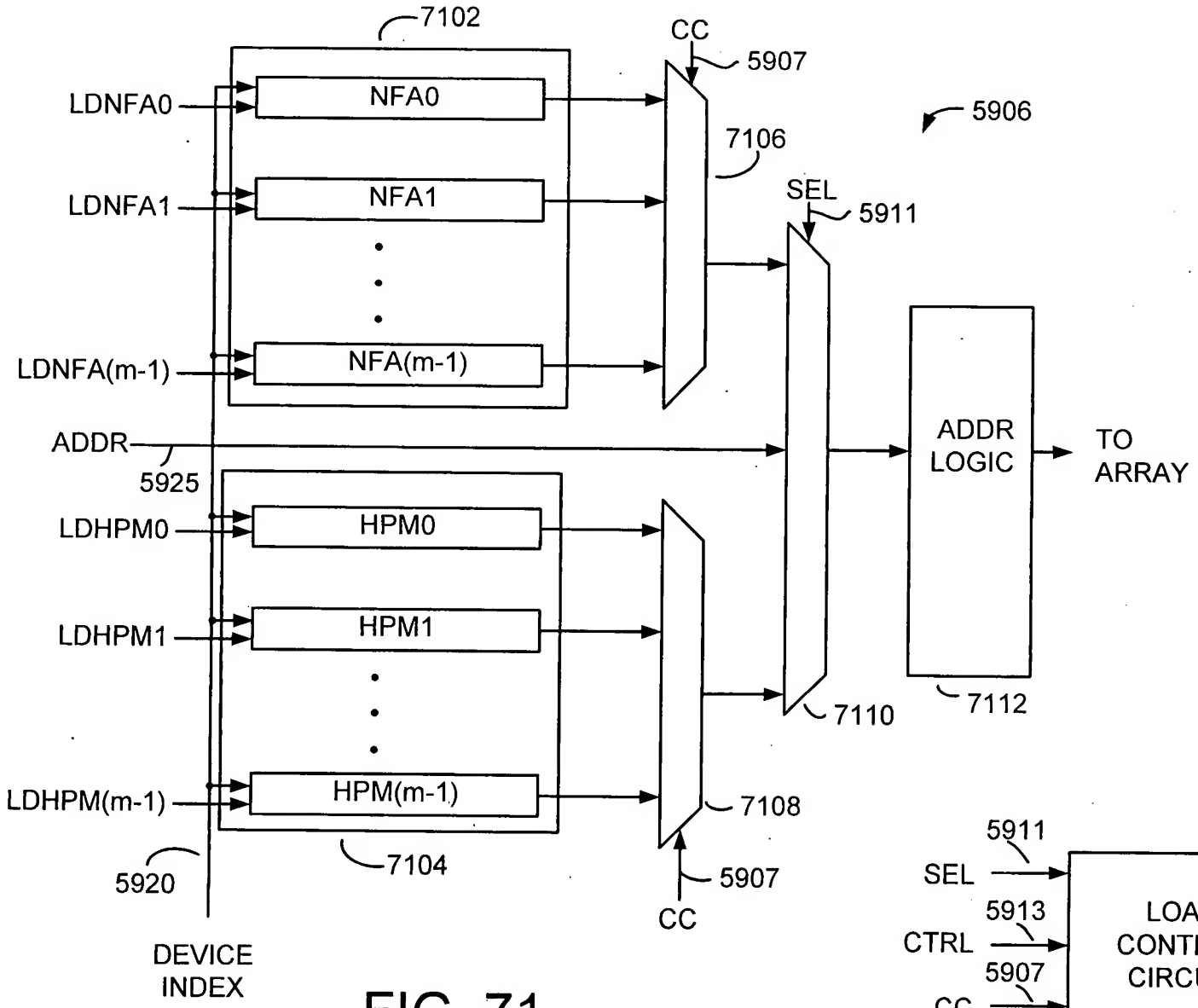

7102
CC
5907
5906
LDNFA0
NFA0
7106
LDNFA1
NFA1
SEL
5911
LDNFA(m-1)
NFA(m-1)
ADDR
5925
ADDR LOGIC
TO ARRAY
LDHPM0
HPM0
LDHPM1
HPM1
7110
7112
LDHPM(m-1)
HPM(m-1)
7108
5920
7104
5907
CC
DEVICE INDEX

FIG. 71

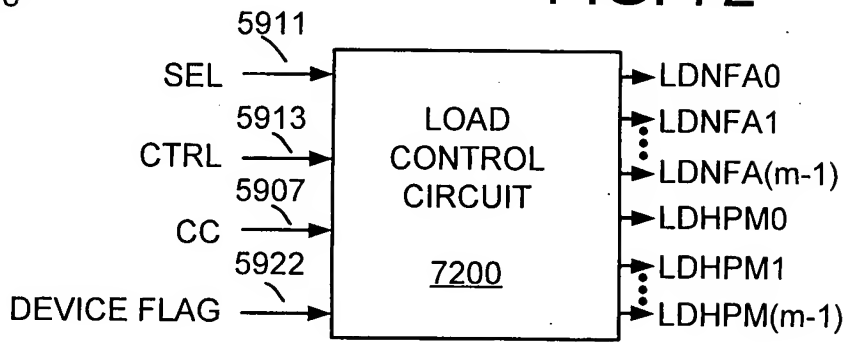

5911
SEL
5913
CTRL
5907
CC
5922
DEVICE FLAG
LOAD CONTROL CIRCUIT
7200
LDNFA0
LDNFA1
LDNFA(m-1)
LDHPM0
LDHPM1
LDHPM(m-1)

FIG. 72

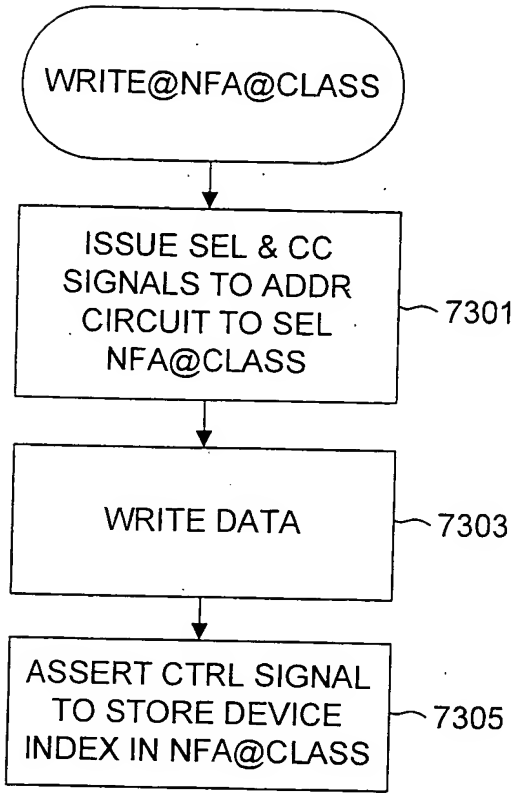


FIG. 73

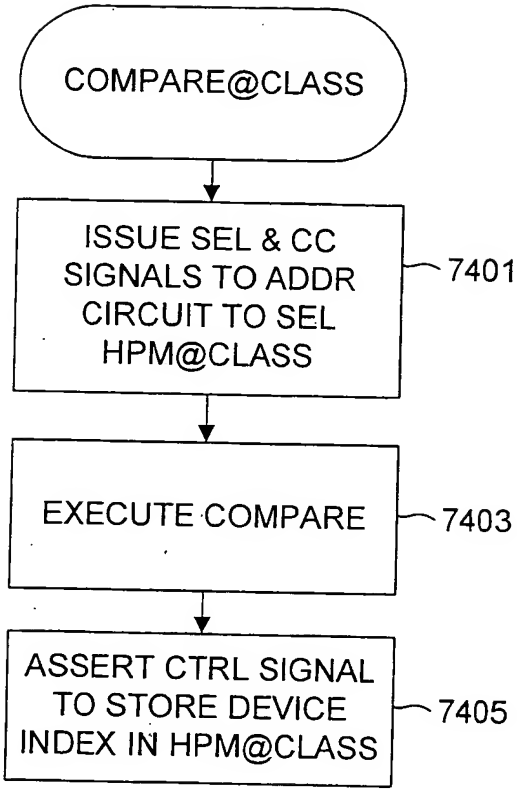


FIG. 74

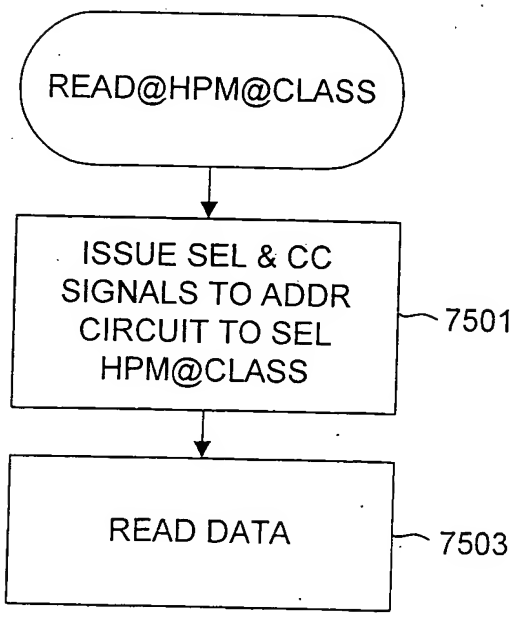


FIG. 75

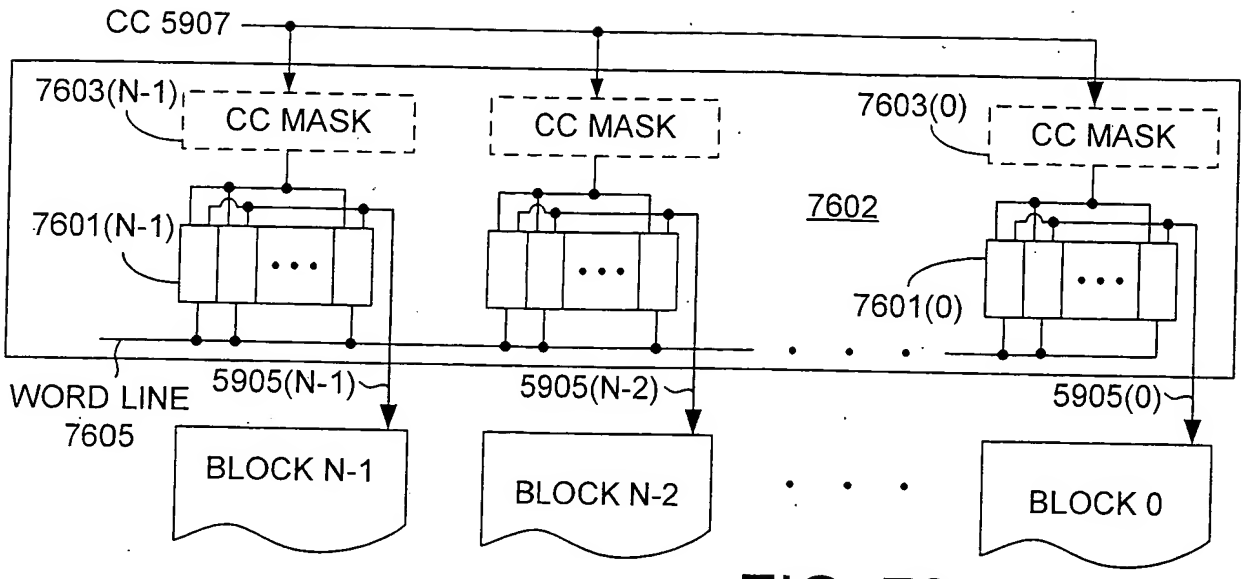

CC 5907
7603(N-1)
CC MASK
CC MASK
7603(0)
CC MASK
7601(N-1)
7602
7601(0)
WORD LINE
7605
5905(N-1)
5905(N-2)
5905(0)
BLOCK N-1
BLOCK N-2
BLOCK 0

FIG. 76

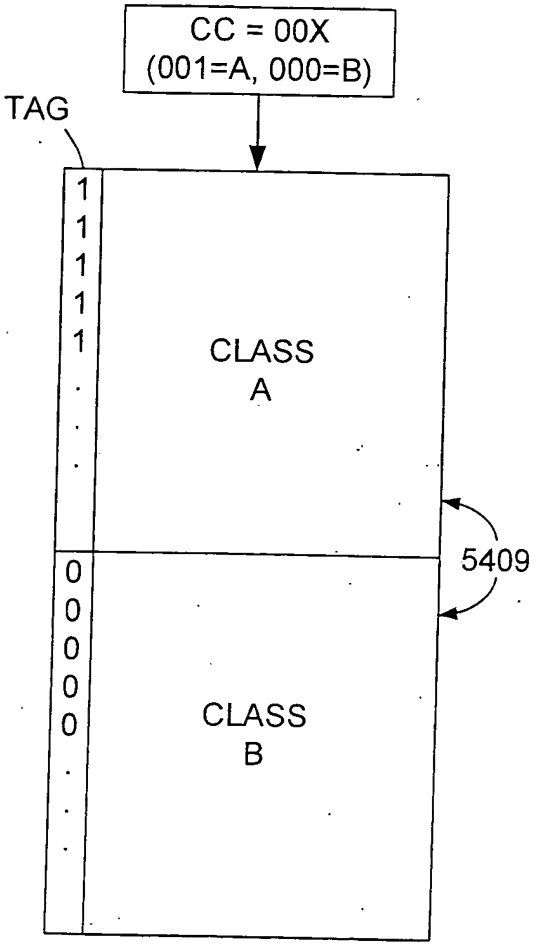

CC = 00X
(001=A, 000=B)
TAG
1
1
1
1
1
CLASS
A
5409
0
0
0
0
0
CLASS
B

FIG. 77